N.Z

FINAL REPORT

MARS SPACECRAFT POWER SYSTEM DEVELOPMENT

CONTRACT NO. 952150

PREPARED FOR

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
4800 OAK GROVE DRIVE
PASADENA, CALIFORNIA 91103

GENERAL ELECTRIC

DOCUMENT NO. 68SD4305
26 JULY 1968

FINAL REPORT

MARS SPACECRAFT POWER SYSTEM DEVELOPMENT

CONTRACT NO. 952150

PREPARED BY:

E. BERKERY
A. KIRPICH
N. KUTNER
R. PELLMANN
M. READ
N. SHEPARD
D. TASCA
D. WEIN

APPROVED BY:

R.P. WOLFSON

W.R. BECRAFT

THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY, AS SPONSORED BY THE NATIONAL AERONAUTICS AND SPACE ADMINISTRATION UNDER CONTRACT NAS7-100.

PREPARED FOR

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
4800 OAK GROVE DRIVE
PASADENA, CALIFORNIA 91103

GENERAL ELECTRIC

MISSILE AND SPACE DIVISION
Valley Forge Space Technology Center
P.O. Box 8555 • Philadelphia 1, Penna.

This report contains information prepared by the General Electric Company under JPL subcontract. Its content is not necessarily endorsed by the Jet Propulsion Laboratory, California Institute of Technology, or the National Aeronautics and Space Administration.

ABSTRACT

This study examined possibilities for improving the performance and reliability of Mariner power systems as they might be applied to future Mars flyby and orbiter missions. A system concept was developed which appears to yield attractive performance and reliability gains and, at the same time, permits use of most of the hardware concepts developed for earlier Mariner power systems. The concept, a modified shunt system, has been analyzed and the results appear to warrant further detailed design, test, and evaluation.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont)

TABLE OF CONTENTS (Cont)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont)

LIST OF ILLUSTRATIONS (Cont)

LIST OF ILLUSTRATIONS (Cont)

LIST OF TABLES

ERRATA FOR:

"Final Report

Mars Spacecraft Power System Development

Contract No. 952150"

GE Document No. 68SD4305

26 July 1968

Page No.	Correction
4-2	Figure 4.1-1 -- Show armature of Earth/Mars mode switch in "E" position
4-2	Figure 4.1-2 -- Ordinate should read: "Error Signal, E ~ $(V_{BUS}-V_{REF})$"
4-11	13th line: "let" should be "leg"
4-13/14	Figure 4.4-1 corrections: - Parentheses for (E') - Remove "MI" from "Main Boost/Inverter/Amplifier Group" title. - 2 Intersection dots missing on Raw DC bus; 1 dot missing between main error and shunt amplifier.
4-24	14th line -- add "s" to element 15th line -- close parenthesis
4-29/30	Table 4.6-1: Line 12 -- Change 56/55 to 37.5/36.7 Line 20 -- Change (17) - .97 + (19) to ((17) - .97) + (19) Line 24 -- Insert - between (1) and 60. Line 25 -- Insert - between (2) and 60.
4-32	14th line: Replace sentence: "This is shown .. " with "This pertains to columns 2, 4, 6, 11 and the left subdivision of columns 8, 10, 12, 13 and 14."
4-33	4th line -- change 1.04 to 1.94
4-34	24th line -- Change Section 4.6.3.2 to Section 4.6.3.3
4-38	Figure 4.6-3: "Temp. Variation per Figure 4.6-2"
4-40	Figure 4.6-4: Label abscissa: "Array Margin (Watts)" Add note to upper right: "Case I, 60° C @ 1.00 AU"
4-52	Line 21: Change °F to °C.
4-58	Line 7: Parenthesize case (a)
4-59	Line 17: Should read..." inch is 0.08..."
4-63	Table 4.7-1: Overload rating for MM'69 should read "376 watts - 0.1 msec"

Page No.	Correction
4-64	Table 4.7-1: - Capitalize MM'69 System - Indent "Main" under Free-run frequency - Charge Regulator Input Voltage should be 53 volts max.
4/65/66	Figure 4.7-2: - Array output line from 4A1 should show (I) 18 current monitor - Label middle upper module "Power Control 4A11"
4-67	Line 20: "span" should be "spar"
4-69	Figure 4.7-4: Six lines leading to test connector should each show diode as in top line.
4-74	Figure 4.7-7: Line from Array bus is hanging -- join to low power Circuit line at left of diode.
4-98	Figure 4.10-2: Base drive resistor of right hand transistor should be joined to Signal from Shunt Amplifier not the Return as shown.
5-26	Figure 5.1.2-3: 3rd number in Total Weight column is missing -- should be 95.6
5-83	Figure 5.1.6-2: Curve 1 -- Z = wLC should read $Z = wL_C$
5-123/124	Figure 5.2.6-3 "x" crossing missing from Inverter output.
5-136	Figure 5.2.9-1 Interchange "Array" and "Battery" titles
5-86	Lines 7 and 8: Place period after "element". Delete "until the lowest element....."
5-89	Equation (5.2.1-4): Lambda subscript should be B, not beta. Other beta(s) to remain.
5-91	Line 8: Change Figure 5.2.4-6 to Figure 5.2.1-6.
5-96	Line 16: Change "circuit" to "configuration."
5-101	Top Figure: Show line between blocks 3 and 4.
5-117/118	Figure 5.2.6-1: 1st block of Condition No. 4 on left should read: "$E_D < E_{D\,MIN}$" 3rd block of Condition No. 5 on left should read: "$E_B > E_{B\,MIN}$

Page No.	Correction
5-125	Line 16: Change "$E_B > E_{B\,MIN}$" to "$E_B < E_{B\,MIN}$"
5-132	Line 20: Change "0.8628" to "0.8626".

SECTION 1

INTRODUCTION AND SUMMARY

This is the final report covering work performed by the General Electric Company for the Jet Propulsion Laboratory under Contract 952150, "Mars Spacecraft Power System Development."

The general objective of this Phase I study was to develop an optimum Mariner-class/Mars power system for application to future flyby and orbiter missions that will provide improved utilization of solar array capacity and greater reliability. The existing Mariner Mars '69 design served as the basis for comparison.

Using load profile requirements for an orbiting mission in the early 1970's, the study resulted in the design of a power system (designated the Shunt System) which offers the desired improvements as summarized below:

	SHUNT SYSTEM	REFERENCE MM'69 SYSTEM
Array Demand	382 watts	410 watts
Array Margin Improvement	28 watts	--------
Power System Weight	120.8 lb	120.5 lb
Reliability		
Full Success	0.86	0.83
Degraded Success	0.93	0.90
Functional Elements Eliminated	Share Booster Share Mode Detector Array Zener Diodes	--------
Functional Elements - New	Earth/Mars Mode Relay Shunt Regulator	--------

Functional Elements with minor modifications	Array Battery Boost Regulator 2.4 KHz Inverter 400 Hz Inverter Power Source Logic Power Control Power Distribution	
Unregulated bus voltage	25 - 38.2 vdc	25 - 50 vdc

The system is very similar to proven Mariner power systems. Full advantage was taken of the development, test, and flight background of the existing Mariner systems, and changes were made only where significant efficiency and/or reliability gain appeared possible.

The additional power available to the load (28 watts) can represent either additional power margin or approximately 25 percent more useful science payload power. When array power becomes marginal -- either through degradation or increased sun distance -- the MM'69 system will go into an undesirable battery-array sharing mode of operation resulting in inefficient array usage and share boost cycling. The shunt system is not faced with this problem and will provide efficient use of full array capacity and minimum battery operation. This advantage is primarily associated with orbiting missions.

A related advantage of the shunt system concerns allowable battery charge rates. In the shunt system, battery charge power is automatically reduced when array power is limited. Consequently, in the shunt system the battery charge rate can be set higher than normally required with the attendant advantage of providing greater operational flexibility, either for obtaining longer orbiting life or for handling a variety of emergency situations. If this higher charge rate were used with the MM'69 system, under similar array limited circumstances, an inefficient sharing mode of operation would result. Again, this advantage is essentially peculiar to the orbiting mission.

The reliability improvement occurs primarily through the elimination of the share mode detector and booster, and the array zener diodes. Block redundancy is used to improve the reliability of the major power conditioning elements and is quite similar to the approach used on the MM'69 system. Evaluation of alternate concepts did not yield significant improvements.

A significant difference between flyby and orbiting missions concerns the available time for science data acquisition. Advantage can be taken of the extended time available in orbiting missions by incorporating additional science load control switches. This can result in reduced peak load demands, more options for science load fault protection, and greater mission flexibility. Consequently, recommendations are made for Phase II Study of additional science relays and science load fault protection for orbiting missions.

The study identified the critical aspects of the power system performance and reliability, and investigated them in considerable detail. Special attention was paid to assessing the interrelationships of the various functional elements from both performance and reliability viewpoints. In two instances laboratory evaluation of key points was undertaken. The study identifies numerous specific tasks which should be pursued during a Phase II detail design and development program in order to realize the potential benefits of the shunt system.

This Final Report discusses all of the effort accomplished by the General Electric Company during the entire performance period of the contract. Accordingly, the contents of the midterm report have been incorporated in this Final Report when it was deemed appropriate. The detailed study objectives, as stated in the Statement of Work, are listed in Table 1-1 along with a cross index of where each requirement is treated in this Final Report.

Table 1-1. Cross-Reference to the Requirements of Contract No. 952150

CONTRACT PARAGRAPH NO.	CONTRACT TASK DESCRIPTION	FINAL REPORT SECTION
(a) (1) (i)	Definition of each model power system studied (Mariner Mars '69 shall be one of the model configurations)	3.0, 4.0, 5.1.1 5.2
(a) (1) (ii)	The analysis of each model power system, including:	See below
(A)	Various voltage regulation methods	5.1.1
(B)	Optimum frequency for ac distribution. What penalties are associated with using 2.4 kHz instead of the optimum frequency?	3.3, 5.1.2
(C)	Concepts of critical and noncritical busses for ac distribution.	4.5, 5.1.5, 6.0
(D)	Optimum battery-charger/battery interface	4.1, 4.6.3.2, 5.3.2
1.	Optimum charge rate	4.6.1, 4.6.2, 4.6.3.2, 4.7.5, 5.3.2.3
2.	Optimum battery charger cutoff voltage	Same as above
3.	Optimum flight sequence for switching battery charger ON & OFF	4.3, 4.6, 4.7, 5.3.2
4.	Optimum method of charging to maximize battery life	4.1, 4.6.3.2 5.3.2
(E)	Providing increased reliability through use of redundancy, failure detection and functional element switching	4.4 and see below
1.	Optimum method of detecting failures with a functional element. How should a failure be defined?	4.4, 5.1.4, 5.2.6

Table 1-1. Cross-Reference to the Requirements of Contract No. 952150 (Cont)

CONTRACT PARAGRAPH NO.	CONTRACT TASK DESCRIPTION	FINAL REPORT SECTION
2.	Failure modes for each functional element and the manifestations of the failures at the input and output terminals	5.1.4
3.	How does a failure in one functional element affect the performance of other functional elements?	4.4.1, 5.1.4, 5.1.5, 5.2.6
4.	Element sizing to ensure that a failure in one element will not lead to the damaging of other elements before the failure is detected, and corrective action is taken.	4.7.8, 4.7.3, 4.7.5, 5.1.5
5.	Methods to ensure that operational elements will not be switched out due to a failure in a relocated functional element	5.1.5, 5.2.1, 5.2.6
6.	Failure detection logic setting and/or re-settling and comparison of the relative merits of automatic and/or ground-commanded failure mode switching circuits	4.4, 4.4.2, 4.4.3, 5.2.6
7.	Methods to protect against failures occurring in other spacecraft systems and consideration of the effect of each method on power system sizing and performance.	4.4.2, 4.5, 5.1.5, 6.0
(a) (1) (iii)	Recommendation of an optimum power system configuration, considering the following criteria:	4.0 and see below
(A)	Elimination of solar array zener diodes	4.0 & 5.1.1
(B)	Elimination of the two stable operating points	4.0 & 5.1.1
(C)	Reduction of voltage swing on the unregulated bus	4.0 & 5.1.1
(D)	Optimization of the ratio of weight to reliability	5.2.9

Table 1-1. Cross-Reference to the Requirements of Contract No. 952150 (Cont)

CONTRACT PARAGRAPH NO.	CONTRACT TASK DESCRIPTION	FINAL REPORT SECTION
(E)	Improvement in the transient response for step changes in loads	4.7.3, 5.1.6
(F)	Improvement in noise rejection in load switching circuitry	5.1.3.5
(G)	Isolation of the command inputs to power system and use of redundant control circuitry to provide fail-safe operation	5.1.3.2, 5.1.3.3 5.1.3.4
(H)	Improved utilization of solar array capacity	4.6
(a) (2)	Determine weight, sizing and parts count and assess the reliability of the recommended system. Present the power and energy design margins. Describe the rationale used in arriving at the particular margins.	4.6, 4.8, 5.2
(a) (3)	Recommend power system telemetry points and parameter ranges for the recommended system configuration. Rank the telemetry channel assignments in order of importance.	4.9.1
(a) (4)	Block diagram each functional element. Determine type of circuits and required redundancy.	2.0 4.4, 4.7, 5.2.9

SECTION 2
STUDY OBJECTIVES AND APPROACH

The prime study objective, as set forth in the contract, was to develop an optimum Mariner-Class spacecraft electrical power system, for both orbiting and flyby missions, which would provide: (a) improved utilization of solar array capability, and (b) greater reliability than the present Mariner Mars power system (Mariner '69 system).

An important element in the GE approach, adopted early in the study, was that the existing Mariner power system was well established and hence any alternative system, or portion thereof, must indicate sufficient improvement in efficiency and/or reliabilility in order to recommend its use. This ground rule was felt to be a dominant one because of:

a. The interplanetary long life success of the Mariner power system

b. The long and continuous development and testing history of the Mariner system.

A second important element in the GE approach was to converge early on the general system concept which appeared to offer the most potential reliability and efficiency improvement, and then to devote the majority of the study to detailed investigation and design of the selected concept. This approach appeared most attractive because of the following:

a. The team undertaking the study was composed of senior personnel having a wealth of background experience in the power system field, particularly for closely related missions. Hence, this team could converge rapidly on the most likely alternate systems.

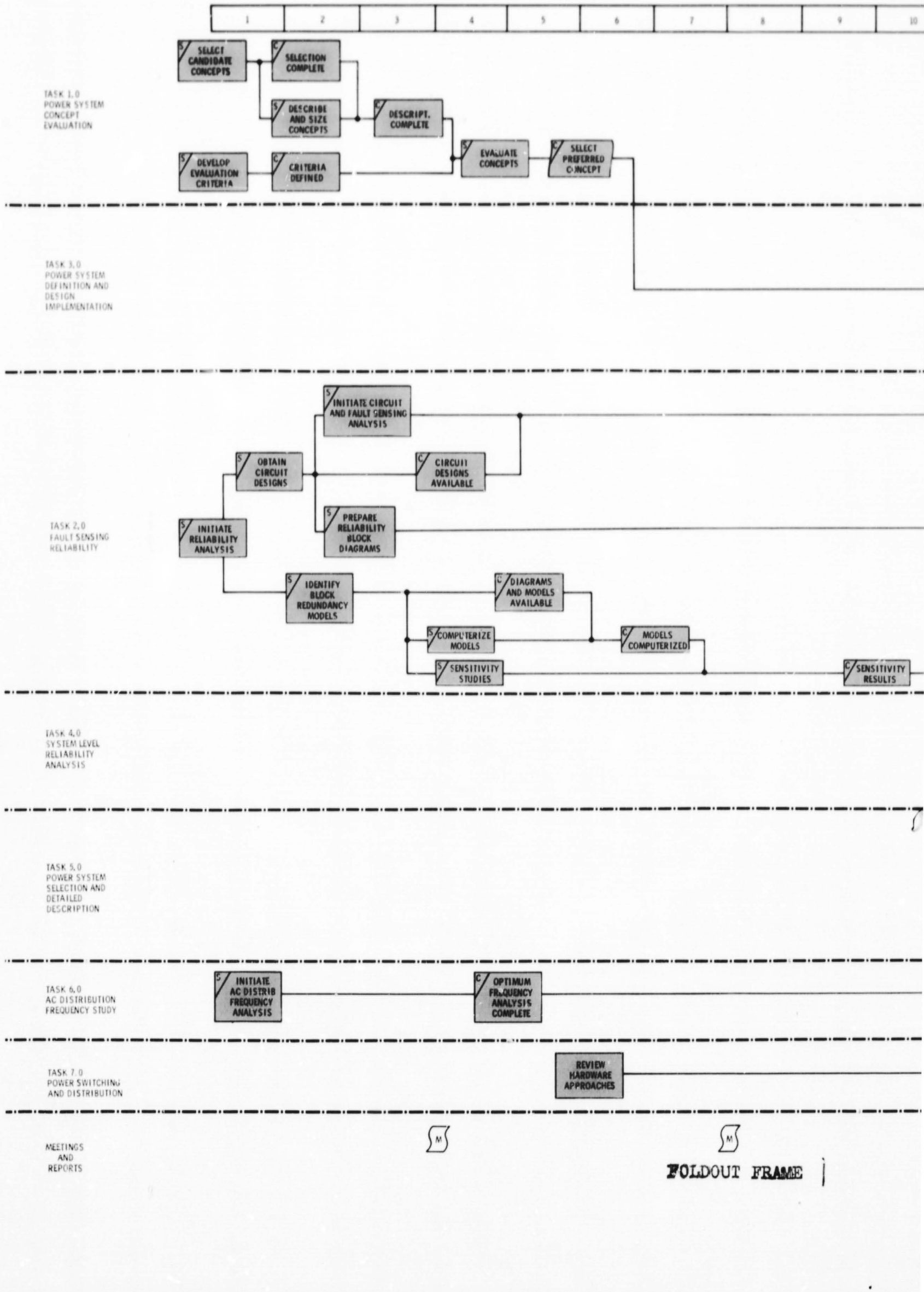
b. The alternate concepts considered were fairly close to the Mariner '69 system from an efficiency and reliability standpoint; none appeared to offer dramatic efficiency or reliability improvements. Consequently, it appeared necessary to throughly investigate the selected concept in order to accurately define its efficiency and reliability.

A third ground rule, based on guidelines and information provided by JPL early in the study, was to concentrate on orbiter missions rather than flyby missions.

The fourth element in the GE approach involved the approach to reliability. The general shortcomings of reliability analysis and prediction were recognized. However, it was decided that significant insight into the operation of the subsystem could be obtained in a relative if not absolute way by using the latest techniques and computer tools to perform reliability sensitivity studies of key aspects of the subsystem. These sensitivity studies, however, were to be combined with failure mode analyses and evaluated on the basis of engineering judgment and experience rather than purely accepting the reliability numbers as conclusive.

The final element in the GE approach was to focus the study on the subsystem level and only consider circuit design where the specifics of the design affected the subsystem level investigation. Black box circuit design, development, and test could then logically be conducted in a Phase II program if desirable.

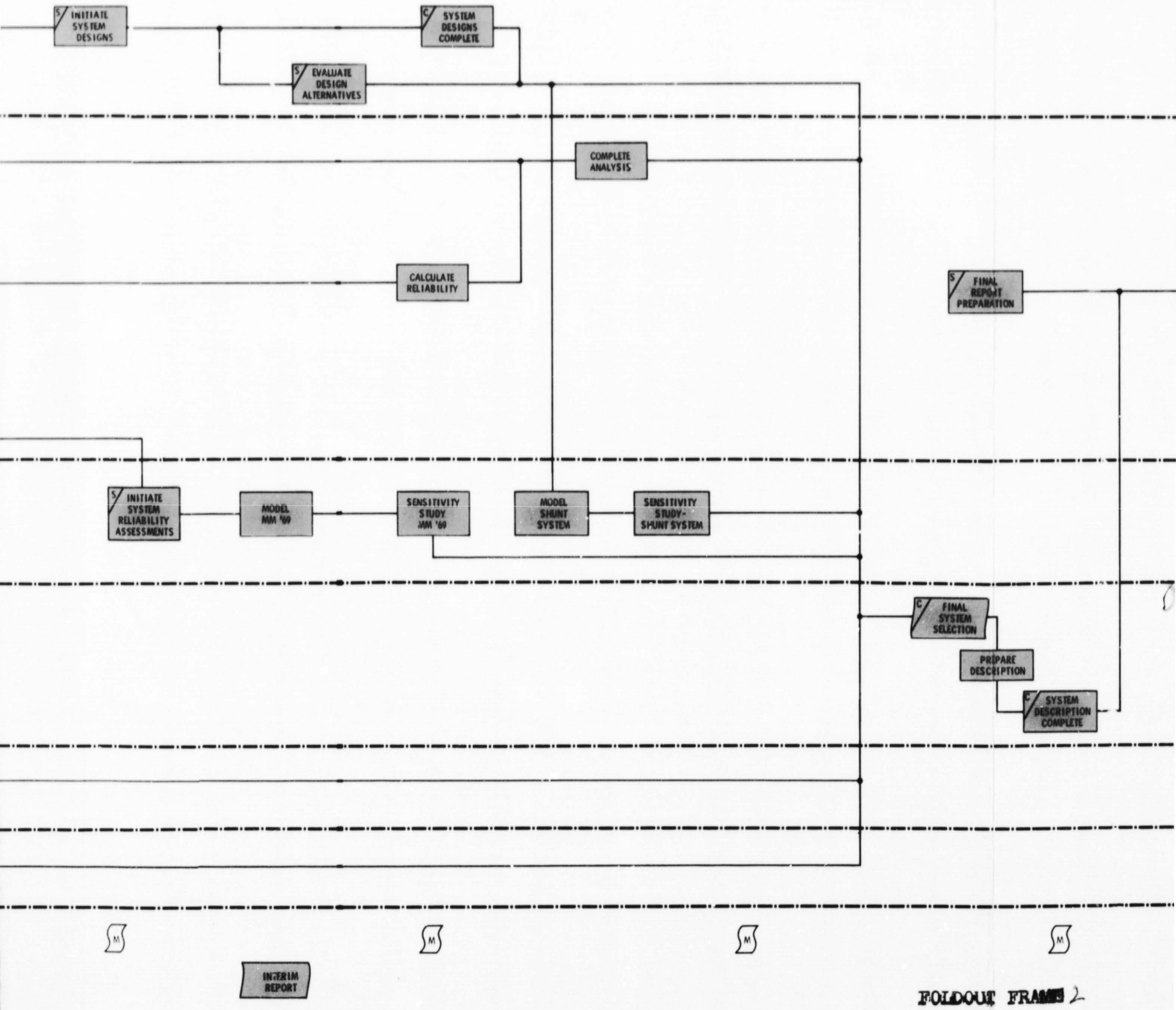
Figure 2-1 shows the Work Flow Diagram followed during the study.



FOLDOUT FRAME

(WEEKS FROM GO AHEAD)

11	12	13	14	15	16	17	18	19	20	21	22	23	24	2



FOLDOUT FRAME 2

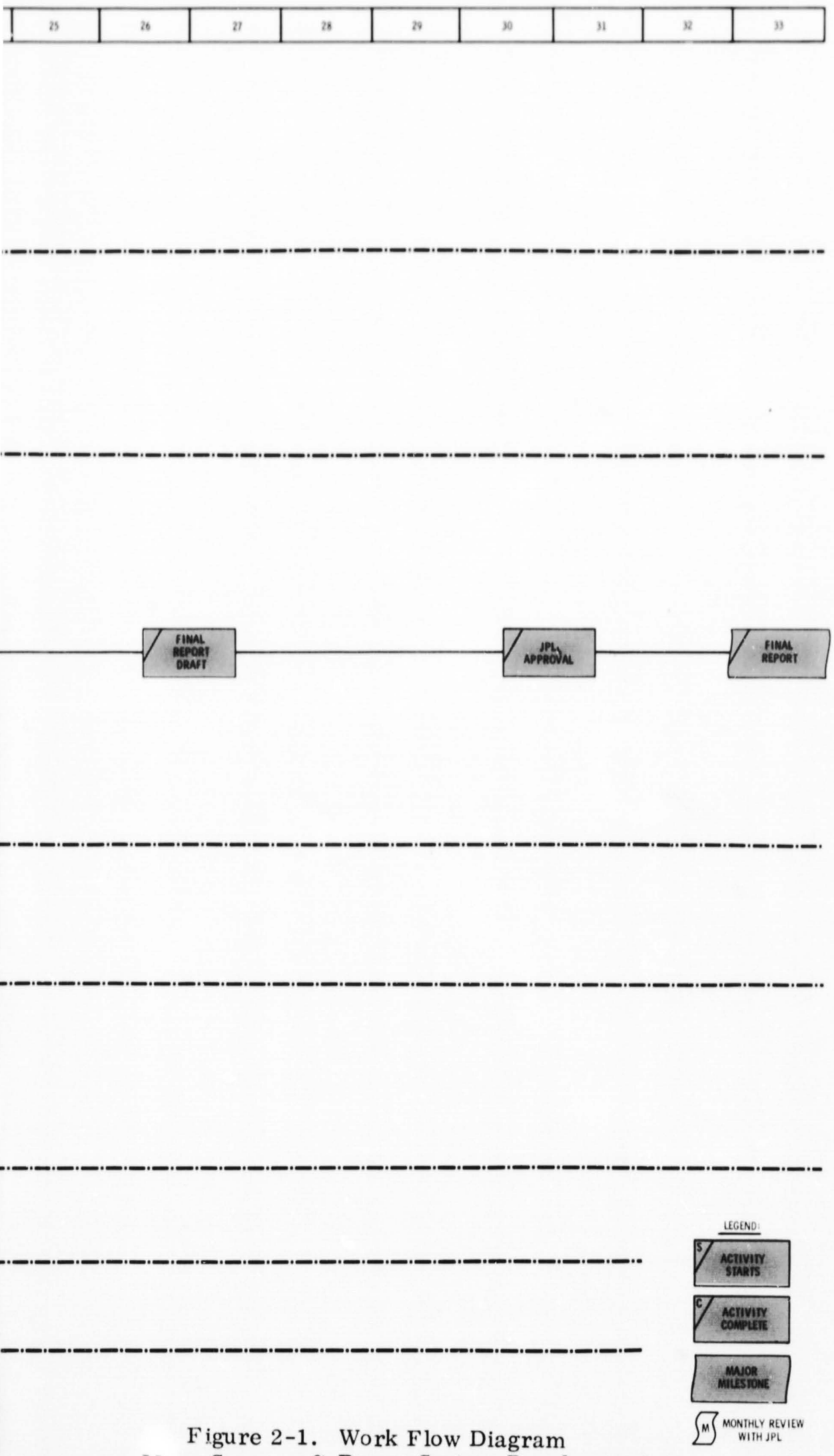


Figure 2-1. Work Flow Diagram
Mars Spacecraft Power System Development

FOLDOUT FRAME 3

SECTION 3

CONSTRAINTS AND GUIDELINES

Guidelines for the study are largely drawn from the requirements for the MM'69 power system and from load profile estimates for typical Mars orbiter missions in the early 1970's. Specific characteristics, either specified or implied, are summarized below.

3.1 POWER SYSTEM TYPE

The power system will utilize solar arrays for power generation and electrochemical batteries for energy storage.

3.2 SOLAR ARRAY ORIENTATION

The solar arrays will be fully sun oriented, except for brief maneuver periods when power will be supplied by the spacecraft batteries.

3.3 DISTRIBUTION

To least disturb the power system interface with other spacecraft subsystems and OSE as presently defined for the MM '69 system, the types of distributed power will be identical to that of the MM '69 system:

Regulated ac power

50 volt rms, single phase, 2.4 kHz

27.2 volt rms, three phase, 400 Hz

28 volt rms, single phase, 400 Hz

Unregulated dc power

25 to 50 volts, extreme limits

3.4 LOAD PROFILE

Typical power requirements by user designation, power type, and mission phase for an orbiting mission have been furnished by JPL and are summarized on Table 3-1.

Table 3-1. Power Requirements (Watts) for Orbiting Mission

POWER FORM	LOAD DESIGNATION	FLIGHT PHASE** ONE(1)*	TWO(3)	THREE(4)	FOUR(4)	FIVE(1)	SIX(6)	SEVEN(1)	EIGHT(2)	NINE(1)	TEN(2)	ELEVEN(2)	TWELVE(6)	THIRTEEN(6)	FOURTEEN(6)
2.4 KHz	DAS	-0.00	-0.00	-0.00	-0.00	-0.00	20.00	-0.00	-0.00	-0.00	-0.00	20.00	-0.00	-0.00	-0.00
	TVS	-0.00	-0.00	-0.00	-0.00	-0.00	32.00	-0.00	-0.00	-0.00	-0.00	32.00	-0.00	-0.00	-0.00
	IRR	-0.00	-0.00	-0.00	-0.00	-0.00	3.00	-0.00	-0.00	-0.00	-0.00	3.00	-0.00	-0.00	-0.00
	IRS	-0.00	-0.00	-0.00	-0.00	-0.00	4.00	-0.00	-0.00	-0.00	-0.00	4.00	-0.00	-0.00	-0.00
	UVS	-0.00	-0.00	-0.00	-0.00	-0.00	12.00	-0.00	-0.00	-0.00	-0.00	12.00	-0.00	-0.00	-0.00
	FTS	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00	15.00
	FCS	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20	3.20
	CC+S	39.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00	19.00
	PYRO	-0.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
	PWRD	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25	2.25
	DSS	21.00	22.00	10.00	10.00	10.00	18.00	10.00	19.00	10.00	10.00	23.00	15.00	19.00	19.00
	A/C1	13.00	25.00	16.00	16.00	23.00	16.00	23.00	16.00	23.00	16.00	23.00	16.00	16.00	18.00
	A/C2	-0.00	-0.00	-0.00	-0.00	10.50	-0.00	10.50	-0.00	10.50	-0.00	-0.00	-0.00	-0.00	-0.00
	SCNE	5.30	5.30	5.30	5.30	5.30	28.50	5.30	5.30	5.30	5.30	16.50	5.30	5.30	5.30
	RFS	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20	32.20
	CYRE	8.00	8.00	8.00	8.00	8.00	8.00	8.00	8.00	8.00	8.00	8.00	8.00	8.00	8.00
	T/C1	50.00	50.00	50.00	50.00	50.00	-0.00	50.00	50.00	50.00	50.00	-0.00	50.00	50.00	50.00
	TOTAL	188.95	182.95	161.95	161.95	179.45	214.15	179.45	170.95	179.45	161.95	207.15	166.95	170.95	169.95
400 Hz, 3Φ	GYRO	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00
	TOTAL	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00
400 Hz, 1Φ	SCNM	-0.00	-0.00	-0.00	-0.00	-0.00	12.00	-0.00	-0.00	-0.00	-0.00	12.00	-0.00	-0.00	-0.00
	IRSM	-0.00	-0.00	-0.00	-0.00	-0.00	3.00	-0.00	-0.00	-0.00	-0.00	3.50	-0.00	-0.00	-0.00
	TOTAL	-0.00	-0.00	-0.00	-0.00	-0.00	12.00	-0.00	-0.00	-0.00	-0.00	15.00	-0.00	-0.00	-0.00
28 VDC	VALV	-0.00	-0.00	-0.00	-0.00	30.00	-0.00	30.00	-0.00	30.00	-0.00	-0.00	-0.00	-0.00	-0.00
	GIMB	-0.00	-0.00	-0.00	-0.00	35.00	-0.00	35.00	-0.00	35.00	-0.00	-0.00	-0.00	-0.00	-0.00
	TOTAL	-0.00	-0.00	-0.00	-0.00	65.00	-0.00	65.00	-0.00	65.00	-0.00	-0.00	-0.00	-0.00	-0.00
25 - 50 VDC	T/C2	7.30	15.00	15.00	15.00	7.30	15.00	7.30	7.30	7.30	7.30	7.30	15.00	15.00	15.00
	T/C3	4.90	10.00	10.00	10.00	4.90	10.00	4.90	4.90	4.90	4.90	4.90	10.00	10.00	10.00
	TWT	55.00	55.00	55.00	55.00	55.00	89.00	89.00	89.00	55.00	55.00	89.00	55.00	89.00	55.00
	BTCG	0.50	0.50	25.00	0.50	0.50	0.50	0.50	25.00	0.50	25.00	0.50	0.50	0.50	0.50
	BRFS	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50
	TOTAL	69.20	82.00	106.50	82.00	69.20	116.00	103.20	127.70	69.20	93.70	103.20	82.00	116.00	82.00

** FLIGHT PHASES

ONE -LAUNCH
TWO -STAR ACQUISITION
THREE -CRUISE I (BATTERY CHARGER ON)
FOUR - CRUISE II (BATTERY CHARGER OFF)
FIVE -MANEUVER
SIX -FAR ENCOUNTER
SEVEN -ORBIT INSERTION
EIGHT -PLAYBACK - FAR ENCOUNTER
NINE -ORBIT TRIM
TEN -ORBIT CRUISE - CC+S UPDATE
ELEVEN -TV SEQUENCE
TWELVE -EARTH OCCULTATION
THIRTEEN -PLAYBACK ATR
FOURTEEN -PLAYBACK DTR

* POWER SUBSYSTEM STATUS

(1) = NORMAL - BATTERY
(2) = GYROS ON - BATTERY
(3) = NORMAL - NEAR EARTH
(4) = GYROS ON - NEAR EARTH
(5) = NORMAL - NEAR MARS
(6) = GYROS ON - NEAR MARS

Table 3-1. Power Requirements (Watts), Orbiting Mission (Cont)

Phase Number	Phase Name	Duration
One	Launch	67 minutes max
Two	Star Acquisition	Not specified
Three	Cruise I (Battery Charger On)	Not specified
Four	Cruise II (Battery Charger Off)	Not specified
Five	Maneuver	84 minutes
Six	Far Encounter	Not specified
Seven	Orbit Insertion	96 minutes
Eight	Playback - Far Encounter	Not specified
Nine	Orbit Trim	84 minutes (Note A)
Ten	Orbit Cruise - CC&S Update	Not specified
Eleven	TV Sequence	60 minutes (assumed)
Twelve	Earth Occultation	Not specified
Thirteen	Playback ATR	162 minutes (assumed)
Fourteen	Playback DTR	24 minutes (assumed)

Notes:

A. 1^{st} orbit trim no sooner than 24 hours after Orbit Insertion; subsequent orbit trims no sooner than 24 hours after previous orbit trim.

B. Time durations during maneuvers are associated with the RS14 engine system.

3.5 TRANSIT AND ORBIT CHARACTERISTICS

Where necessary for sizing and evaluation, a specific launch opportunity was examined in order to use realistic times. The opportunity examined corresponded to a 1971 opportunity, as shown below; however, the study is general for Mars orbiting missions in the early 1970's.

Transit time: 6 to 8 months

Arrival date: 14 November 1971

Orbit period: 12 hours

Onset of Solar Occultations: 130 days after arrival

Length of Solar Occultations: up to 90 minutes

3.6 RELIABILITY IMPROVEMENT*

a. "Wherever the weight, cost, and schedule risk penalties are not prohibitive, functional or alternate mode redundancy should be employed such that no single failure mode of any electronic or electrical mechanical component could cause a catastrophic effect on the mission".

b. "Particular emphasis shall be placed upon simple and conservative design . . ."

*Mariner Mars 1969 Spacecraft Design Criteria No. M69-2-100, 19 September 1967, JPL

SECTION 4

SYSTEM DESCRIPTION

The orbiting load profile and mission definition described earlier served as the basis for developing the power system design. A trade study of possible configurations was completed about midway through the program and resulted in the selection of a shunt regulation system. The considerations and principal results of this trade study were presented in the Interim Report and are repeated in Section 5.1.1 of this report. Further definition and modifications have been made to the original selection upon careful review of operational conditions. The recommended system is described below.

4.1 SIMPLIFIED BLOCK DIAGRAM

A simplified block diagram of the shunt regulation system is shown in Figure 4.1-1. Inverter power (2.4 kHz and 400 Hz inverters) is derived from the regulated dc bus. The dc regulation is maintained by controlling the shunt regulators, the battery charge regulator and the boost regulator in response to separate regions of the error amplifier input as shown on Figure 4.1-2. The shunt regulator operates in the highest error region with maximum solar array shunting in response to error e_4 down to no shunting at e_3. At this point the available array power at the regulated voltage just satisfies the load demand along with any battery charging that may be underway. Upon further load demands or decreased array power, the array power used for battery charging is first diverted to the load before battery discharge power is called for. This occurs in response to the e_3 to e_2 error region. With further load demands or further decreases in array power, the boost regulator supplies battery power in response to the error level in the e_2 to e_1 region.

The required sensitivity of the regulator functions (shunt, boost and charge regulators) to different error bands was viewed with some concern during the early study phases. Because the shunt system generally appeared to offer improved performance margins over other configuration candidates (see Section 5.1.1), it was decided to verify the feasibility of regulator sequencing by construction and test of a breadboard. This was accomplished

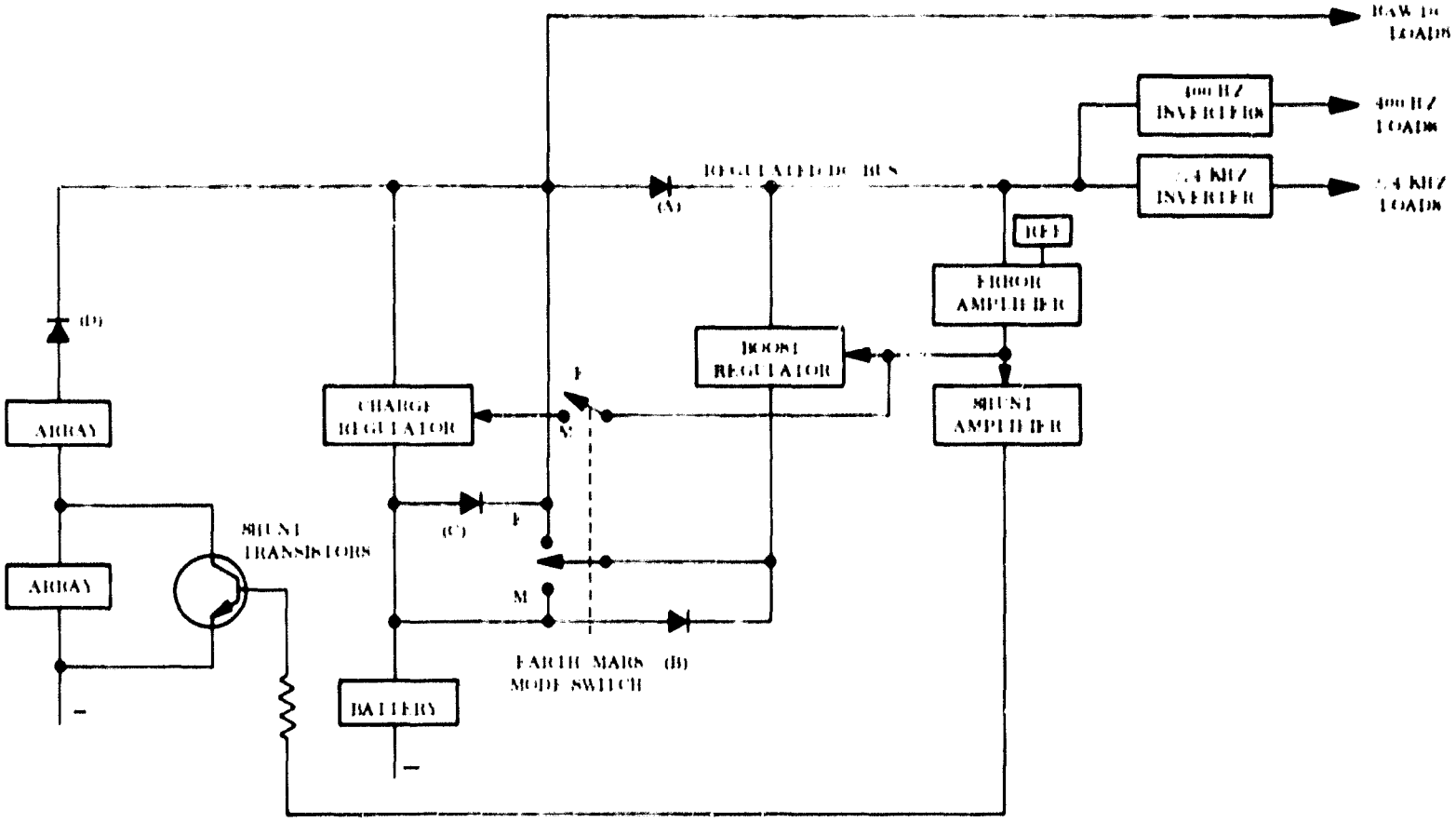


Figure 4.1-1. Simplified Block Diagram Shunt System

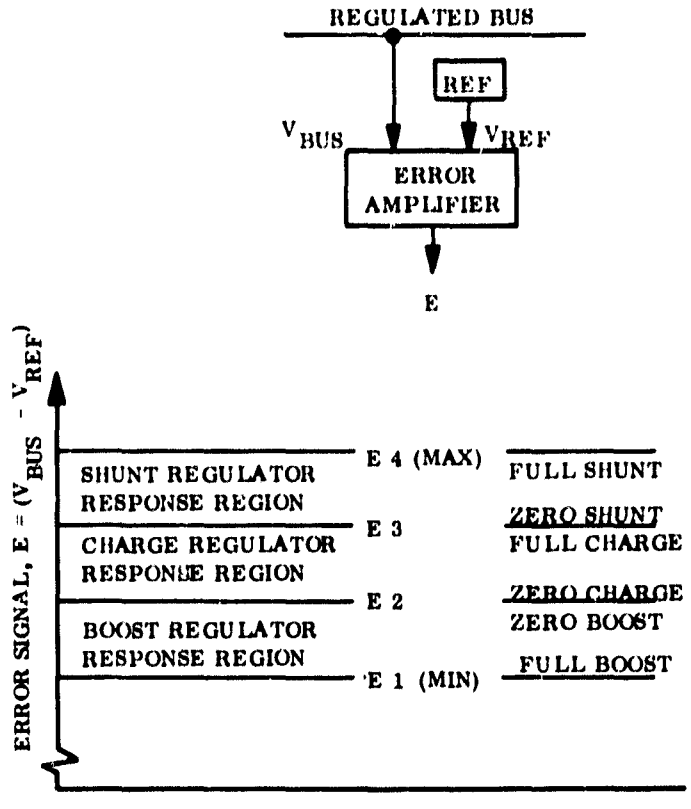


Figure 4.1-2. Response Regions of Shunt, Boost and Charge Regulators

successfully without any significant difficulties. As long as a single error amplifier is used to provide the driving functions, no problems of overlapping sensitivity were evident. A minor step change in the output bus voltage (approximately 1 percent) occurred as the system mode of operation moved between battery charge and battery discharge. The step is due to noise generated at the booster choke input filter in combination with circuit nonlinearities effectively modifying the transfer function of the error detector. The problem can be eliminated by filter modification and designing greater noise immunity into the error detector.

The block diagram (Figure 4.1-1) shows an in-line diode (A) between the array output bus and the regulated bus and the use of an Earth/Mars mode switch. The purpose of this combination is to get around solar array matching problems which arise in the transfer orbit from Earth to Mars. Essentially, the Earth to Mars change in solar array voltage-current characteristics makes it difficult to mutually satisfy near-Earth and near-Mars power requirements at a single array source voltage.

The power-voltage solar array curves of Figure 4.1-3 illustrate the nature of this problem. These curves are based on the use of solar cells having relatively square V-I characteristics, similar to those used on the Mariner '69 solar panels. The factors used in generating these curves and the general question of system sensitivity to solar array performance uncertainties are discussed later in Section 4.6.3. Referring to the P-V curve at 1.5 AU, which is typical of the sun distance for a Mars mission 90 days after encounter, the normalized voltage for maximum power is 1.3. If the system regulated voltage is selected at this level, no power is available from the near-Earth 1.0 AU P-V characteristic. By reducing the normalized voltage to 1.2, equivalent power can be obtained for the 1.5 and 1.0 AU conditions but with a sacrifice in the potential 1.5 AU power of about 6 percent.

The in-line diode (A) and Earth/Mars mode switch solve this problem in the following fashion. During launch and the early cruise phase, the switch is set in the Earth-mode "E" position. In this position the switch contacts are arranged to: (a) introduce raw array power directly to the boost regulator input; (b) insert a blocking diode (B) between the battery and boost regulator input; and (c) disable the battery charge regulator override signal from the error amplifier. No modification to the shunt or boost regulator responses to the error amplifier

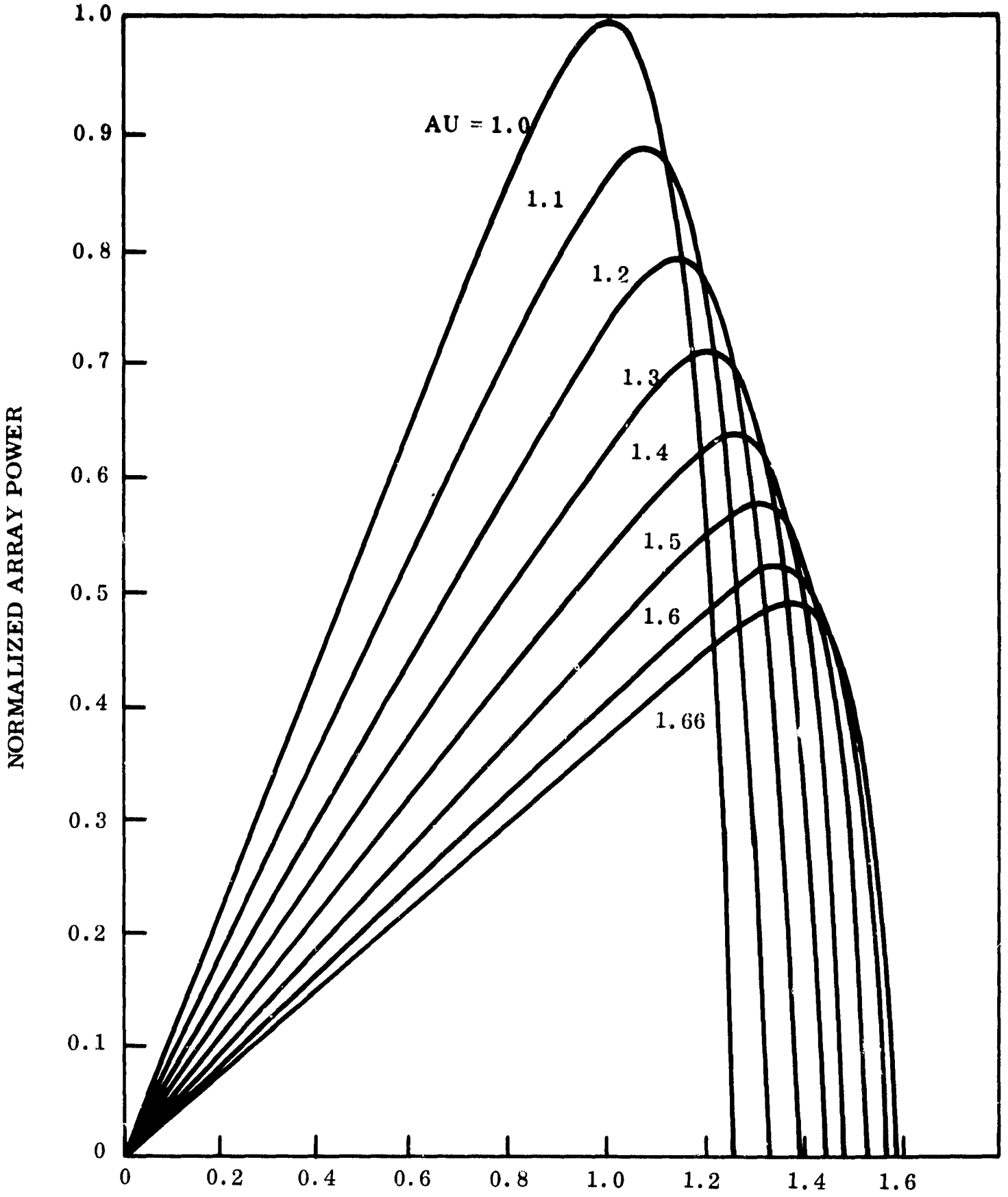


Figure 4.1-3. Predicted Mariner '69 Solar Array P-V Curves

are necessary in the Earth-mode switch position. If array voltage is low, the boost regulator operates to maintain voltage regulation. If array voltage is high, system voltage is maintained by the shunt regulator and array current flows directly through the main in-line diode (A). In either case the battery discharge diodes, (C) and (B), are backbiased.

About 2 months after launch, the change in the solar array voltage-current characteristics permits a transfer of the Earth/Mars mode switch to the "M" position. This has the effect of preventing direct solar array input to the boost regulator and, as will be explained later, avoids the occurrence of array/battery load sharing.

In the "M" position it is possible to provide contact closure around the main in-line diode (A) between the array bus and the regulated bus to gain a slight increase in system efficiency. However, this would not permit isolation of the raw power loads and would result in voltage depression of the regulated bus to the battery discharge level during battery demand periods. As suggested in the Interim Report, an alternative is to use double isolation diodes for each section of the solar array in the manner shown in Figure 4.1-4. Upon review of this approach,

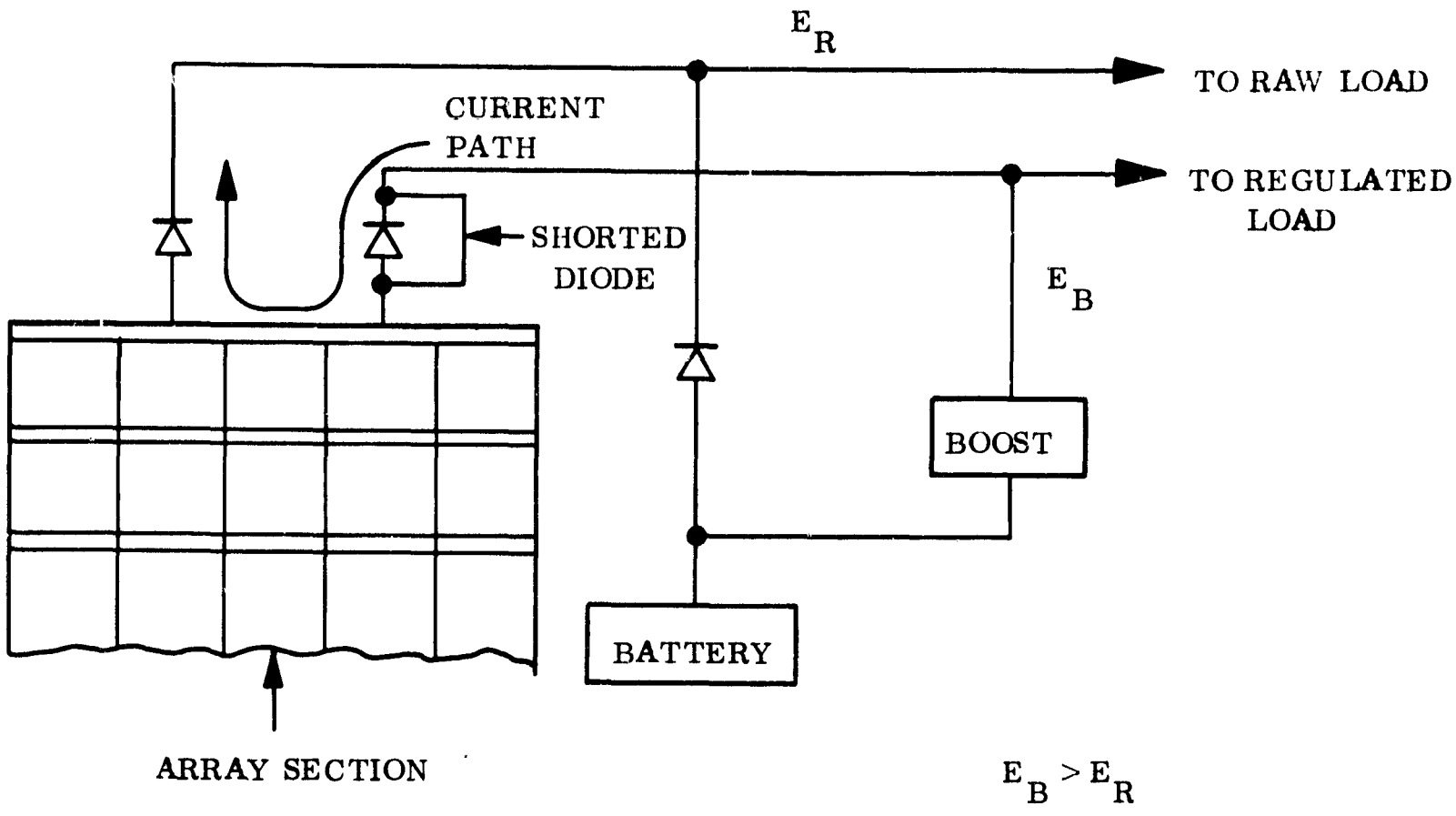


Figure 4.1-4. Array Isolation Diode Failure Mode

it was realized that a short-circuit of one of these diodes could have serious consequences. During normal battery discharge sequences, the raw bus is set at the battery discharge voltage minus the diode drop. With a shorted diode, as shown in Figure 4.1-4, the current path is in a forward direction with respect to the companion diode. The raw load would therefore draw power from the boost regulator possibly exceeding its load rating. Since there are many such isolation diodes, the probability of this failure mode is increased. This approach was therefore dropped in favor of accepting a system inefficiency associated with not providing contact closure around the main in-line diode (A) in Figure 4.1-1.

The shunt regulator for the selected system consists of a shunt amplifier which drives multiple shunt transistor elements located on the solar array. With the use of the MM '69 solar panels, containing 78 series solar cell elements, each shunt transistor is wired across the first 35 elements of each solar cell string. This selection of a "partial" shunt regulator over a full shunt regulator was based on reduced heat dissipation within the shunt elements. The predicted performance is described in Section 4.6 and the specific details of implementation are described in Section 4.7.

In relation to voltage levels and capacity requirements, the battery for the selected system is identical to the MM '69 silver-zinc battery. Some design modification may be required to adapt this battery for an orbiter mission since the battery is required during orbit insertion and orbit trim maneuvers, whereas in flyby missions it only serves as a backup beyond the last midcourse maneuver. The life requirements are actually not too different. For example, in the MM '69 mission the last midcourse maneuver may occur as late as four months after launch, while the transit time is typically about six months. In-house tests on silver-zinc cells which closely match the weight and capacity characteristics of the MM '69 battery cells indicate adequate stand life and subsequent cycle life capability. It is therefore judged that silver-zinc batteries will be adequate for the missions considered in this study. Further discussions on battery considerations are contained in Sections 4.4.6, 4.7.6, and 5.3.2.

The selected charge regulator is also identical to the MM '69 regulator in the sense of being a series dissipative type. Besides on-off control by ground command, a two-step charge

mode is recommended. In the primary mode, charging proceeds at a current limit of 2.0 amperes until a level of 35 volts is reached (1.94 volts per cell). The current decreases thereafter as determined by the battery characteristics, while the regulator maintains a voltage limit of 35 volts. When the current drops to 50 milliamperes, the regulator voltage limit is reduced to 33.6 volts in its secondary mode of operation. This reduces its rate of trickle charging and serves as a backup to ground command turn-off of the regulator.

4.2 SYSTEM VOLTAGES

A guideline used in developing the shunt system was that the forms of distributed power be identical to those of the MM '69 power system. This pertains principally to the 2.4 kHz and 400 Hz supplies. A specific objective was to reduce the range of raw dc power as long as the reduced range is within the existing MM '69 limits (25 to 50 vdc).

In attempting to meet these conditions with the shunt system, it is desirable to take advantage of equipment already developed for the MM '69 system as long as this does not penalize the potential performance gains of the shunt system. Within this framework several options were examined:

Option 1

- Use the existing MM '69 solar array design. Attempt incorporation of shunt regulator elements without disturbing the layout of the solar cells or the panel structure.
- Select battery voltages that match those of the existing MM '69 battery and would permit its use depending on sizing and life requirements.
- Design the boost regulator and inverters to match the shunt regulated voltage which corresponds to the optimum array voltage in near-Mars conditions.

Option 2

- Use the existing MM '69 boost regulator and inverter set to operate at 56 vdc (level at boost regulator output and inverter input).
- Design the solar array for an optimum voltage of 56 vdc (neglecting diode drops) in near-Mars space.
- Design the battery to reduce the range of raw dc voltage.

Essentially, Option 1 proposes that minimal changes be made to the solar array and battery systems with the principal modifications made to the conditioning equipment, and Option 2 proposes the reverse. In evaluating the relative merits of these options, it was concluded that Option 1 is more sensible for the following reasons:

a. More extensive development efforts are associated with solar array and battery designs.

b. Sizing calculations for the solar array and battery (see Section 4.6) indicate that the MM '69 array area and battery capacity are suitable for the particular orbiter mission examined, and it is possible to consider their use in this mission.

c. The implied changes to the conditioning equipment are not extensive in design concept and principally involve changes in the design of magnetic components.

Thus, Option 1 was selected as the basis for further development of the design. The optimum voltage of the MM '69 solar panels then serve to establish the boost regulator output level and the input level of the inverters after proper allowance is made for diode voltage drops.

As will be shown in the analysis of array sensitivity, Section 4.6.3.1, the optimum array voltage is 38 to 39 volts with a slight dependence on the sun distance after Mars encounter. This voltage takes the solar array isolation diode losses, (D) in Figure 4.1-1, into account. Allowing a drop of 0.8 volts through the main in-line diode (A) the nominal voltage required at the boost regulator output is about 37.5 volts.

The MM '69 battery contains 18 silver-zinc cells in series. At a voltage limit of 1.94 volts per cell, the maximum charge regulator output voltage is 35 volts which results in a drop of 3 to 4 volts through the regulator during shunt regulator operation. This provides sufficient margin to permit battery charging in the near-Earth mode of operation with array power fed directly to the boost regulator input. In fact, during this mode of operation the relative array, charge regulator, and battery voltages are completely identical to those planned for the MM '69 system.

4.3 OPERATIONAL SEQUENCE

The operating characteristics of the power system as configured in Figure 4.1-1 are described below for the principal mission phases.

4.3.1 PRELAUNCH

After ground checkout and the transfer to internal power, the Earth/Mars mode switch is set in the Earth mode position. Battery power is supplied to the input of the boost regulator and to the raw power bus at the battery discharge voltage of about 25 to 30 volts.

4.3.2 LAUNCH TO SOLAR ACQUISITION

The system continues to operate on battery power. The solar panels are deployed sometime prior to the solar acquisition sequence. They may be deployed during a solar occultation phase depending on launch and transfer trajectory parameters, and will cool to an extent determined by the length of occultation. If lower temperatures (possibly down to minus $200^{o}F$) exist at the time of solar acquisition, the array will furnish power directly to the regulated bus through the main in-line diode (A) in Figure 4.1-1, with excess power dissipated in the solar array shunt transistors. Under this circumstance, the error amplifier signal prevents boost regulator operation.

4.3.3 EARLY CRUISE

Soon after solar acquisition, or possibly during the acquisition sequence itself, the panels will reach their near-Earth equilibrium temperature of around $140^{o}F$. Solar panel power will be available at voltages lower than the regulated level and the system will revert to boost regulator operation. The array voltage is, however, greater than the battery charge voltage (35 volts maximum based on an 18 cell battery with 1.94 volts/cell for charging) and battery recharging can proceed through command actuation of the charge regulator. After an appropriate time lapse, on the order of 12 hours, the battery is fully recharged and the charger is deactivated by ground command. Failure to deactivate is backed up by voltage and current limiting controls of the charger itself. Beyond this the system operates in the normal boost mode.

4.3.4 MIDCOURSE MANEUVERS

Assuming no partial illumination of the panels during maneuvers, the system operates on battery power identically to that described for the launch phase. With partial array illumination, not sufficient to satisfy the entire load, the array voltage is drawn down to the battery discharge voltage and power is supplied in a sharing mode. With solar reacquisition, recharging is initiated as described earlier.

4.3.5 MIDCRUISE TO LATE CRUISE

About 2 months after launch, the increased sun distance will result in reduced panel temperatures that would permit transfer to the Mars mode of operation, i.e., transferring the Earth/Mars switch to the "M" position. This occurs when the steady state array voltage results in power transfer through the main in-line diode (A). The switch transfer does not modify system operation in any way at this time; in fact the transfer is made without any current flow through the switch contacts. The reason for the transfer is to avoid solar array/battery load sharing during later phases when array power capability is limited. (This condition will be described later for such phases.) The time for switching to the Mars mode of operation is not critical as long as it is done some reasonable time before array power limitations are expected. The switch transfer is accomplished automatically with the CC&S subsystem with ground command backup. Note that in Figure 4.1-1 the Mars mode switch position eliminates the direct supply of array power to the boost regulator, eliminates the battery discharge diode, (B), to the boost regulator by shortcircuiting the diode, and introduces override capability to the charge regulator from the error amplifier.

4.3.6 ORBIT INSERTION AND ORBIT TRIMS

Assuming no partial illumination of the solar array during these maneuvers, the system operates on battery power. Raw power is supplied through the diode leg (C) of the battery discharge circuit and to the boost regulator through the second leg. Before describing operation during solar reacquisition at the end of these maneuvers, consider that the Earth/Mars switch is in the "E" position and that the solar array is marginally able to provide the required power under full illumination. To put some numbers on this, assume the net array demand is 380 watts and the array can produce 380 watts with some slight excess. During battery

discharge the array is clamped at the battery discharge voltage at around 25 to 30 volts. As solar reacquisition proceeds, the solar array contributes an increasing amount of current at this clamped discharge voltage. Only about 75 percent of the maximum power is available with operation at 25 to 30 volts compared to ideal operation at 39 volts. Figure 4.1-3 illustrates this by the comparison of power for a normalized voltage of 1.25 corresponding to 39 volts and a normalized voltage range of 0.80 to 0.96 corresponding to 25 to 30 volts. Thus, at the time of full solar reacquisition, the potential array power is unavailable and battery discharge continues. This condition may be corrected by a momentary boost of battery voltage, by a momentary load reduction, or by a Mars switch as described below.

Consider now a similar situation with the Earth/Mars switch in the "M" position. Again during battery discharge, the array is clamped at the battery discharge voltage. The significant difference is that only a small portion of the total power supplied passes through the battery discharge let through diode (C) to which the array voltage is clamped. This power is used by the raw loads and has a maximum value of about 115 watts. Thus, when the array power at 25 to 30 volts exceeds 115 watts, battery discharge through the raw power leg is terminated. With a further slight increase in array power, a step change in array voltage occurs to that level at which power is supplied through the in-line diode, (A), to the regulated bus. With the step change additional array power is made available over and above that used by the raw loads. The system responds by a reduction in boost regulator power further reducing the battery demand. With further buildup of array power, the boost regulator output is first reduced to zero, battery recharge power is next made available and, finally, any excess array power is handled by the shunt regulator. The approach described above explains the need for the Earth/Mars mode switch, and its use eliminates the need for a share boost detector and share booster.

4.3.7 MARS ORBIT PHASE

Operation during this phase is similar to that described for Late Cruise. If solar occultations are encountered, operation is similar to that described for Orbit Insertion.

4.4 REDUNDANCY AND FAULT PROTECTION

The use of redundancy for the selected system is identified on the more detailed block diagram of Figure 4.4-1. The various applications are discussed below.

4.4.1 BOOST/INVERTER/AMPLIFIER GROUP (BIA)

The principal application of switched redundancy concerns the functional group consisting of the following:

a. Main in-line diode between the array and regulated dc bus (A) or (A') in Figure 4.4-1.

b. Boost regulator

c. Voltage reference and error amplifier

d. Shunt regulator amplifier

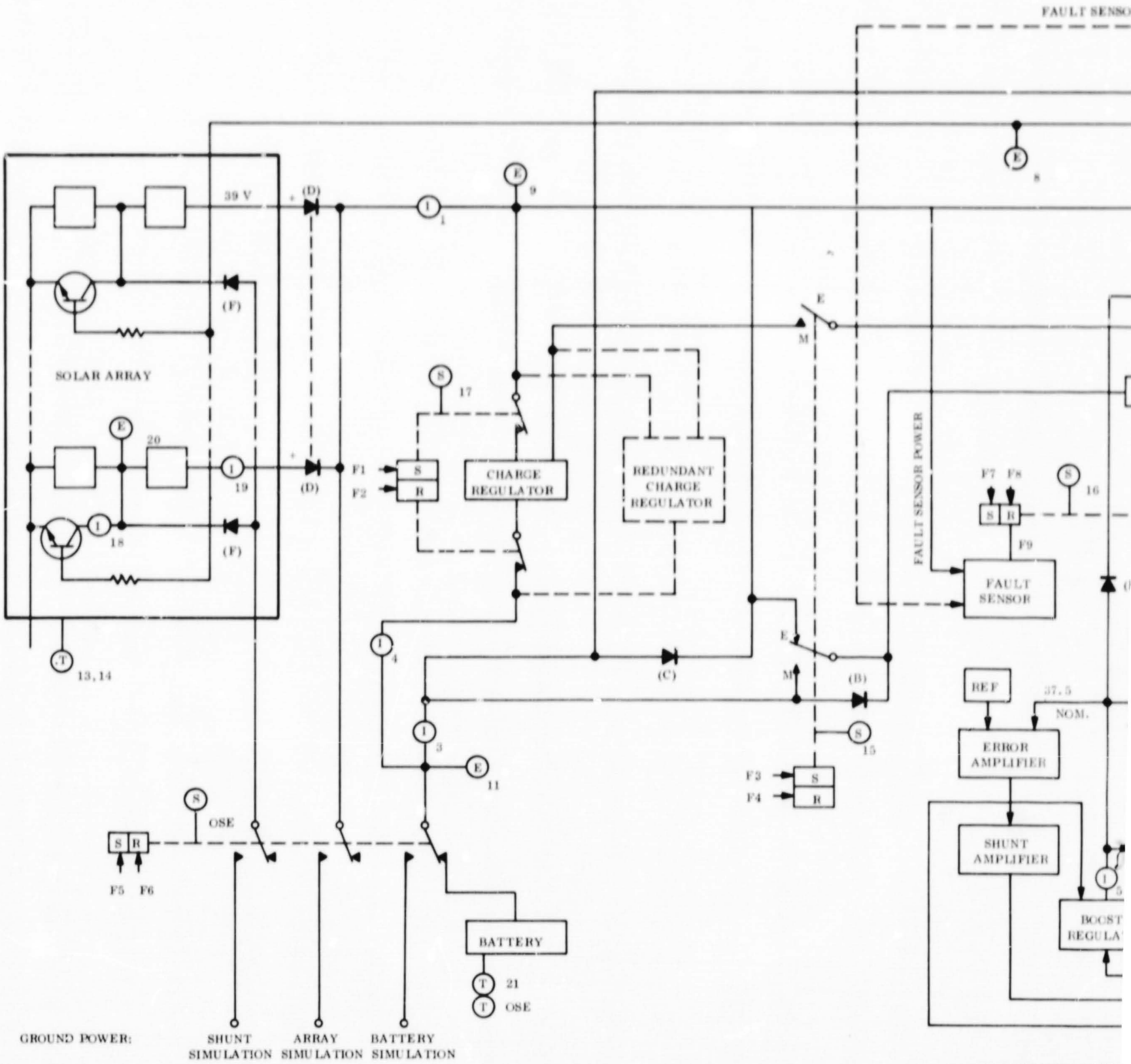
e. 2.4 kHz inverter and clock

A fault sensor monitors the performance of this group as shown on Figure 4.4-1 and transfers operation to an identical group in response to the conditions indicated on Figure 4.4-2.

This redundancy and fault sensor scheme are similar to that used on the MM '69 system. Shunt voltage and battery current fault sensor monitors are tentatively added to identify a possible failure mode that might not appear as an output voltage deviation. This particular condition is simultaneous boost regulator and shunt regulator operation which results in inefficient system operation. If the boost regulator is drawing battery power, it is obvious that any shunting of solar array power is wasteful. The monitors are designed to detect this condition which could arise from a shift in shunt amplifier characteristics or faulty response of the boost regulator.

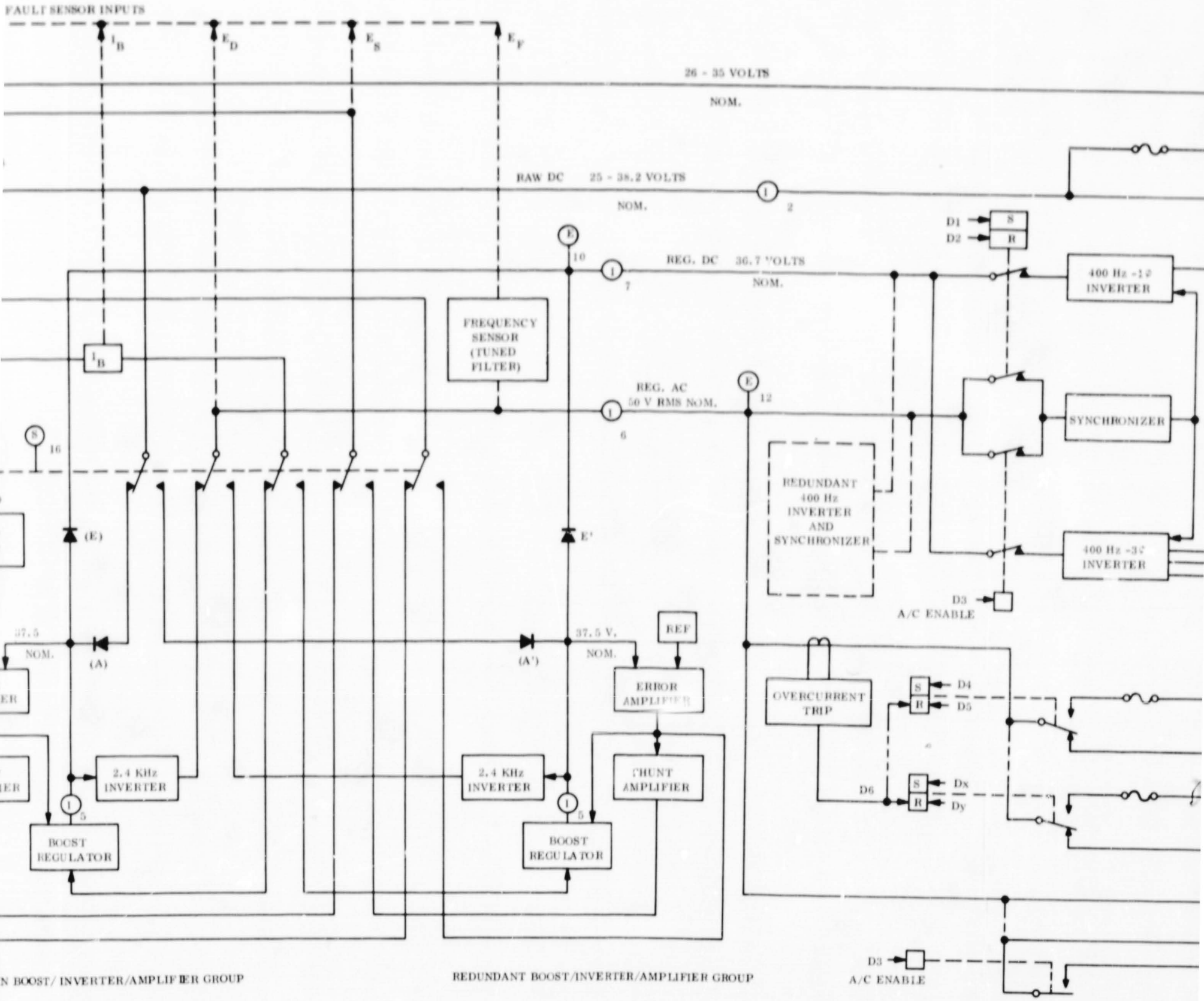
Several alternative schemes were examined in which functions were separately monitored and switched. As described in Section 5.2.6, the alternative schemes were more complicated (see Section 3.6) and none provided a sufficient reliability advantage over the selected approach.

FOLDOUT FRAME 1



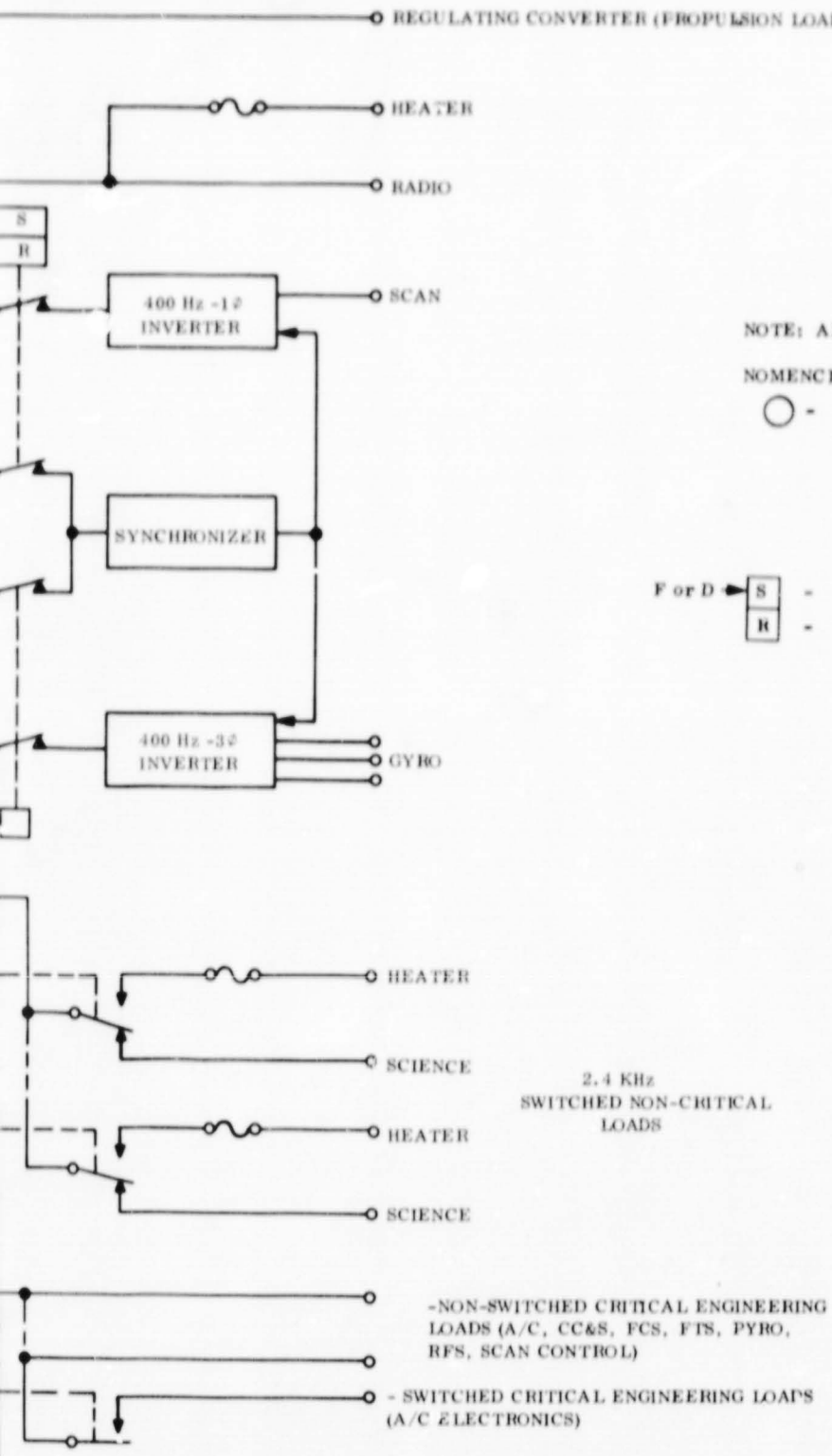
FOLDOUT FRAME

FOLDOUT FRAME 2



FOLDOUT FRAME

FOLDOUT FRAME 3



NOTE: ALL RELAYS SHOWN IN SET POSITION

NOMENCLATURE:

○ - TELEMETRY POINT
E - VOLTAGE
I - CURRENT
T - TEMPERATURE
S - SWITCH STATE
SUBSCRIPT REFERS TO ITEM NO. IN TABLE 4.9.1-1.

F or D → S - RELAY SET POSITION

R - RELAY RESET POSITION

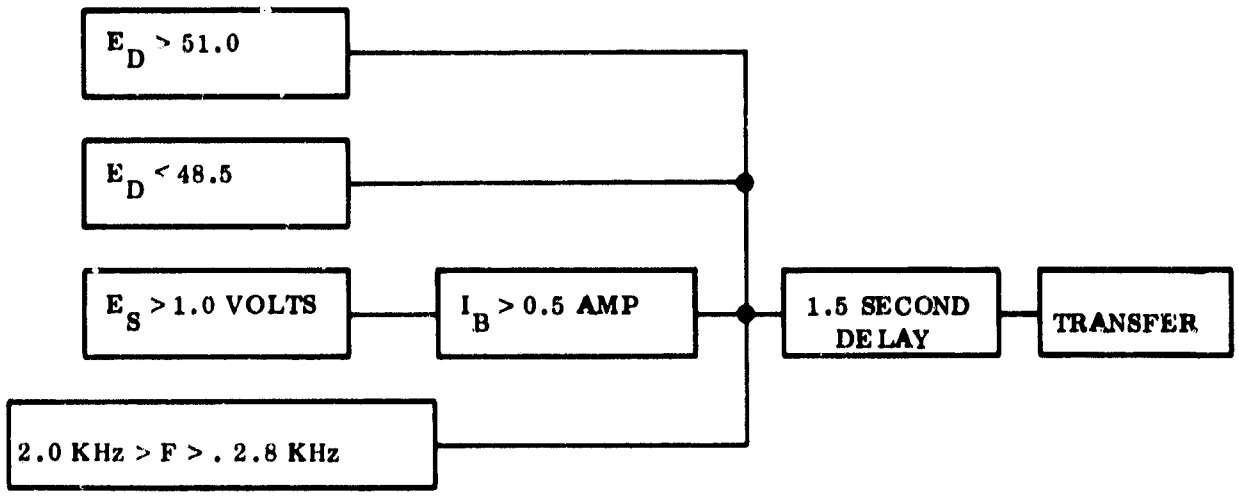
F - COMMAND FOR POWER SYSTEM FUNCTION

D - COMMAND FOR POWER DISTRIBUTION

SUBSCRIPT REFERS TO ITEM NO. IN TABLE 4.9.2-1.

Figure 4.4-1. Shunt System Block Diagram

LDOUT FRAME



NOMENCLATURE:

E_D: DISTRIBUTED 2.4 KHz VOLTAGE. $^{+1.0}_{-1.5}$ VOLTS
NORMAL RANGE : 50 VOLTS RMS

E_S: SHUNT AMPLIFIER VOLTAGE SHUNT TRANSISTORS CONDUCT FOR $E_S > 1.0$ VOLT AND ARE FULL ON AT $E_S \approx 4.7$ VOLTS.

I_B: BOOST REGULATOR INPUT CURRENT

F: DISTRIBUTION FREQUENCY OF 2.4 KHz BUS

Figure 4.4-2. Boost/Inverter/Amplifier Fault Sensor Response

The clock is considered as an integral part of the 2.4 kHz inverter. Clock failure sensing is identical to that used on the MM '69 system and is accomplished by sensing the voltage of a tuned filter at the output of the inverter. If this voltage decreases below a selected level, indicating mismatch of the driving and resonant frequencies, transfer to the redundant unit is initiated. For startup purposes, the inverter is designed to free run in the absence of a clock signal. After the clock is started the inverter operates at the clock frequency. Thus, to detect a clock failure the free run frequency is set at a higher easily discriminated frequency (2.8 kHz). The standby inverter on the other hand is set to free run at 2.4 kHz in the event of failure of the standby clock. This general approach can detect coarse changes in frequency that would result from discrete failures within the digital circuitry of the clock countdown chain. It is not appropriate for sensing small frequency shifts that might arise from slight changes in the crystal oscillator characteristics. In this case resort to majority-vote logic or comparison with another frequency source of comparable accuracy would be necessary. Such techniques are probably not necessary since the dominant failure modes are probably

associated with discrete piece part failure. A more detailed examination of this problem would be warranted during a Phase II effort.

Several alternatives for detecting coarse frequency changes were examined but none appeared to offer significant advantage over the present approach, especially in the light of its existing development and hardware status.

To prevent possible damage to the BIA as a result of external load faults, several protection features are required. In particular, failure of fused loads supplied by the 2.4 kHz inverter incur this requirement. The tolerance in fuse performance may be such that inverter ratings might be dangerously exceeded. For this reason a current limiting protective circuit is recommended. Conversely, fuse ratings must be sufficiently small to fall within the inverter current limit capability.

The boost regulator may also require a current limit form of protection against load faults. Such faults may arise from failures of the 400 Hz inverter, the only other load supplied by the boost regulator aside from the 2.4 kHz inverter. This need will depend on whether and how redundancy is applied to the 400 Hz inverter (see discussion in Section 4.4.2).

Regarding another possible interaction problem, several changes in the routing of signals between the 2.4 kHz inverter and 400 Hz inverter are suggested as shown on Figure 4.4-3. In the present arrangement, failure of the 2.4 kHz power stage could result in the total or partial loss of a driving signal to the 400 Hz synchronizer and could cause damage to the 400 Hz inverter power transistor because regulated power is still applied. Although the 2.4 kHz inverter failure would be rectified by transfer to the redundant BIA, the 400 Hz inverter might be permanently damaged. By deriving the synchronizer signal from the clock or free-run oscillator, this condition is avoided. The supply of clock and free-run oscillator power from the input side of the inverter rather than the output side provides further assurance against this interaction failure condition. Note that failure of input power to the 2.4 kHz inverter also implies loss of power to the 400 Hz inverter and hence, failure of the latter would not occur.

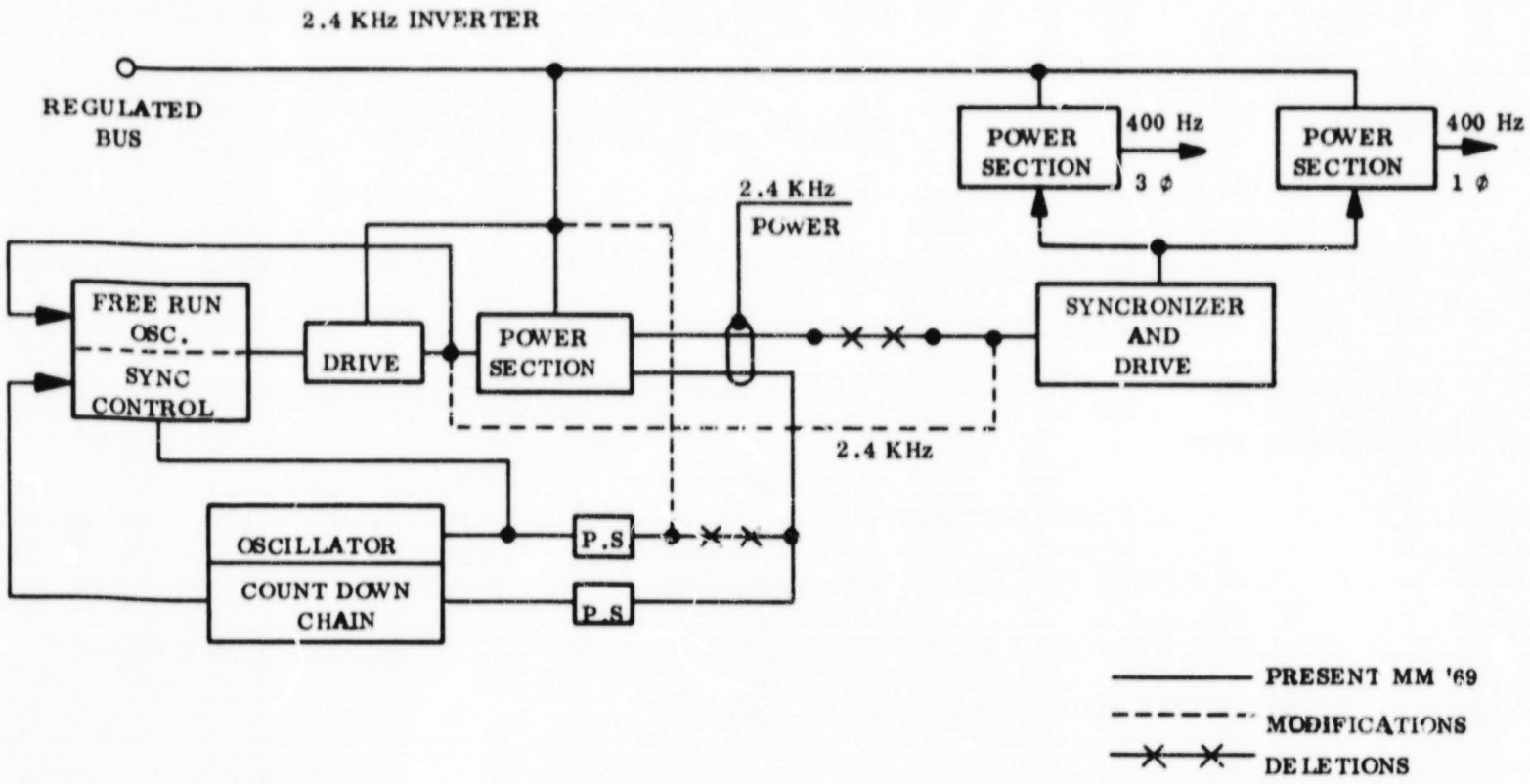


Figure 4.4-3. 2.4 kHz - 400 Hz Inverter Interface

4.4.2 400 Hz INVERTER (SINGLE AND THREE PHASE)

The optional use of redundancy for this function is indicated by the dotted line blocks in Figure 4.4-1. Since this inverter supplies specialized motor loads (gyros, scan drive), it was not possible to determine the need for a redundant inverter without considering load redundancy. Thus, relative reliability evaluations, at the spacecraft system level, might indicate a nonredundant inverter with redundant gyros provides the best overall combination or vice versa.

Reliability evaluation of the 400 Hz inverter indicated the synchronizer was the weakest element. As indicated in Section 5.2.9, an appropriate reliability increase is possible by operating the synchronizer only during the periods of inverter power demand. The extent of circuit modifications that might be required has not been defined sufficiently to permit a firm recommendation.

Although these questions cannot be resolved within the scope of this study, as they involve spacecraft system trade studies, several observations are worth pointing out if redundant inverters are considered. First, it does not appear necessary to incorporate automatic on-board failure detection and switchover. Telemetry information and ground command switchover are most likely sufficient for this purpose. The reason for this is that the inverter supplies motor loads and would most likely fail at the time of startup when current stresses are highest. In the case of the gyros (3-phase power), they are started many hours before their actual operational use. It is reasonable to assume that any necessary switchover could be accomplished in sufficient time by ground command. This argument is even more compelling if the gyros are operated continuously during the mission, a possibility suggested by the development of high reliability air bearing gyros. Since the actual operational periods of gyros during the entire mission are extremely small, the likelihood of a failure during such periods would also be extremely small.

In the case of scan drive motors (single phase power), the startup argument may not be valid since motor startup and shutdown may be an inherent operational characteristic during a scan sequence. For an orbiter mission, loss of the inverter during such a sequence would result in the loss of data associated with that sequence only--switchover by ground command would correct this condition for subsequent scan sequences. For a flyby mission, there would probably be insufficient time to make the redundant transfer by ground command, and for this specific case automatic on-board transfer might be desirable.

The implied avoidance of automatic transfer represents a desire to reduce complexity. As noted later in Section 5.2.6 concerning redundancy options for the boost/inverter/amplifier group, fault sensors can become functionally complex and can very rapidly contribute to unreliability. In the case of the boost/inverter/amplifier, automatic transfer was necessary since only short power outage times can be tolerated by the associated loads. For the 400 Hz inverter, however, the previous rationale provides a basis for avoiding automatic transfer in most cases.

The ability to use ground command switchover depends on the nature of the 400 Hz inverter failure or its associated loads. Open circuit failures do not present a problem in this regard. Short circuit failures, on the other hand, may jeopardize the rest of the system because of sustained heavy current demands. As shown on the block diagram (Figure 4.4-1), the boost regulator could supply the current up to the point of its full duty cycle capability besides that supplied by the solar array directly. Depending on the severity of the load fault, the boost regulator rating might be exceeded. If some form of current limiting circuitry were installed in the regulator for its own self-protection, it is likely that voltage regulation would not be maintained. Thus, until the fault were cleared, the system would be outside its normal limits. If the fault persisted, it is likely that transfer to the redundant BIA would occur, although none of the main BIA elements were faulty.

Fuses located at the input of the prime 400 Hz inverter (not the redundant one) could be used to alleviate this condition. As described in Sections 5.1.4 and 5.1.5, the fuse may be significantly oversized and still clear the fault in much less time than the delay time associated with the BIA fault sensor. In other words, the BIA voltage deviation can be kept sufficiently short in time to prevent redundant transfer.

4.4.3 CHARGE REGULATOR

Redundancy for the charge regulator is also considered in an optional sense. Because of its limited period of operation during the mission, reliability calculations indicate satisfactory values in comparison with other system functions. However, considering the guideline that no single piece part failure shall jeopardize system operation, redundancy might be applicable for this function. If redundancy is used, ground command control provides an adequate method of implementation as in the case of the 400 Hz inverter. Since the interim period between successive battery uses is appreciable (not less than 24 hours), there is no immediacy in transferring to the redundant charger.

If a redundant charge regulator is used, an open circuit failure can be easily detected and corrected by ground command control. A short-circuit failure can cause serious problems depending on solar array power capability at the time of failure. If the array power is only

slightly greater than the load demands, its current will flow through the shorted regulator to the boost regulator input. Any excess current would go toward battery charging. If the array excess is large, the rate of overcharging would be accordingly high with possible damage to the battery. Again, a fuse at the charge regulator input could be used in this situation.

Aside from the question of redundancy, the recommended charge regulator design itself incorporates several backup features. As mentioned, the charger is turned off after full charge is reached after each battery use. This is accomplished by ground command control upon interpretation of telemetry information. Failure to turn the regulator off is backed up by circuit features which reduce the charge voltage to a level correpsonding to the battery open circuit voltage after full charge is reached. This reduces any subsequent overcharge stress. This feature is described in more detail in Section 4.7.5.

4.4.4 SHUNT REGULATOR

Redundancy is separately considered below for the shunt amplifier and shunt transistor dissipative portions of the shunt regulator.

4.4.4.1 Shunt Amplifier

As described earlier, the shunt amplifier is included as part of the boost/inverter/amplifier group (see Section 4.4.1). An alternative to block redundancy was the use of multiple units such that the loss of array power associated with some failures could be tolerated. Of all the logical combinations, shown in Table 4.4-1, all but the first three were discarded because of the requirement for either failure detectors for each amplifier or additional telemetry and command capability to remove failed elements.

Table 4.4-1. Alternate Number of Amplifiers

No. of Amplifiers
1
1 of 2
23 of 24
3 of 4
6 of 8
9 of 12

A relative reliability and weight comparison for the three selected cases is shown in Table 4.4-2.

Table 4.4-2. No. of Amplifiers Evaluated

Total No. of Amplifiers	No. of Amplifiers Required	Weight (lb)	Reliability (Amplifiers Only)
1 No Redundancy	1	0.64	0.9941*
2 Block Redundancy	1	1.50	0.9999
24 Cooperative Multi-Channel Redundancy	23	3.80	0.9911

Because of its higher reliability and the convenience of incorporating it into the boost/inverter/amplifier group, the block redundancy approach was adopted.

4.4.4.2 Shunt Regulator Transistors

Redundancy for the shunt transistors, which form the power dissipation section of the shunt regulator, is provided by their multiple use at the partial tap points of the 24 solar array sections. One transistor is used per section.

Considering transistor open circuit failures, redundancy is implied in the fact that six such failures could occur without affecting system regulation. The analysis leading to this conclusion is described in Section 4.6.4.4.

Considering short circuit failures, redundancy is implied in the fact that the associated loss of array power is restricted to those sections with the failed transistors. The use of resistor isolation at the base of each transistor prevents any effect to the remaining

* As described in Section 5.2.5, the failure rate for the shunt amplifier is 0.09085%/1000 hrs. For a 6500-hr mission, this is equivalent to the reliability of 0.9941 as shown.

transistors. The loss of one of the 24 sections appears acceptable in terms of the array margin estimated in Section 4.6 and is therefore used for the reliability analyses in Sections 5.2.5 and 5.2.7.

An attractive method for decreasing the probability of power loss due to transistor short-circuit failures, the most likely failure modes, is to use two series transistors for each of the 24 array sections with a common drive circuit as shown in Figure 4.4-4. A short circuit failure of either transistor still permits proper operation and would not result in the loss of power of the associated array section. This circuit was briefly examined in the laboratory with satisfactory results. Short circuit failures were simulated for each transistor and in each case the companion transistor performed properly. Since the additional transistors would mean a weight penalty of about 1.5 pounds, it was decided to defer the selection of this approach pending further evaluation during a possible Phase II effort.

4.4.5 DISTRIBUTION

This function contains the numerous relays, relay drivers, and fault protection devices associated with the distribution and control of power to the various loads.

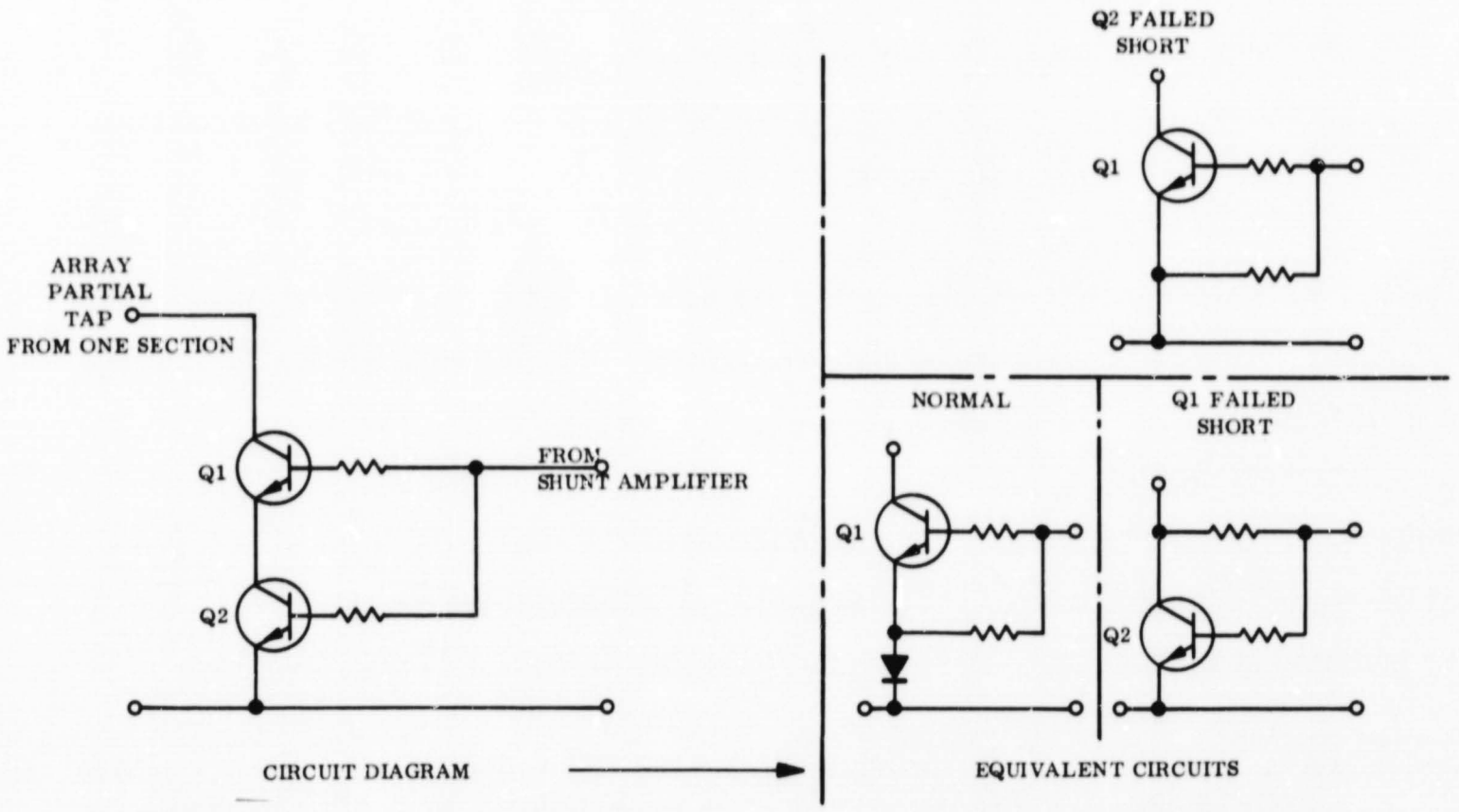


Figure 4.4-4. Piece Part Redundancy of Shunt Dissipator Transistors

In the sense that power distribution design involves many system interfaces, it was not possible to determine where and how specific redundancy features should be applied. Instead, as described in Section 5.1.3, general guidelines have been provided for achieving flexibility, command input redundancy, noise suppression and other desirable distribution characteristics. Specific recommendations are not set forth at this time as implementation of some of these guidelines should be predicated on evaluation of various hardware designs during a Phase II effort.

4.4.6 BATTERY

Considering reserve capacity as a form of redundancy, the battery used in the MM '69 power system is also adequate for the shunt system. As indicated in the system sizing analysis (Section 4.6.1), the maximum demand is 590 watt-hours required during orbit insertion which represents a 47 percent depth of discharge for the battery which is conservatively rated at 1250 watt-hours.

Assuming that the use of two batteries of the MM '69 type would be prohibitive from a weight standpoint, there is the possibility of using two smaller batteries each having half the capacity of the MM '69 battery. This might provide some reliability advantage in that energy demands could still possibly be fulfilled if one of the batteries failed catastrophically. There are, of course, certain drawbacks in this approach:

a. Overall battery weight would be increased by about 10 to 15 percent.

b. A second charge regulator would be required along with additional command and telemetry channels.

c. Most important--advantage could not be taken of the long development, manufacturing, and test experience associated with the battery cells used on the MM '69 battery.

d. Catastrophic battery failures are generally associated with time dependent electrochemical phenomena. There is no reason to believe that the use of two batteries would suffer less in this respect. Certain catastrophic failures might result from faulty manufacture, but it is reasonable to assume that these would be detected through quality assurance test programs.

For the above reasons, the use of separate smaller batteries does not appear warranted for the principal orbiter mission studied in this program.

4.4.7 SOLAR ARRAY

Redundancy is inherent in solar array designs in that multiple current paths are provided in the event of individual solar cell failures. The selected design is based on using the MM '69 solar panels which incorporates such features along with multiple solar cell string isolation diodes.

4.4.8 PIECE PART VERSUS BLACK BOX REDUNDANCY

Aside from the block redundancy (black box redundancy) approaches discussed thus far, piece part redundancy within complex circuit functions provides another approach for increasing reliability. The principal advantage of piece part redundancy is the potential elimination of fault sensor and switchover functions. Its principal disadvantages are: (a) added power consumption, particularly where quad arrangements are used, (b) the difficulty of applying such techniques to various circuit element, and (c) the difficulty of testing (e.g., determining if one diode of a parallel pair is open.

The black box redundancy approach has been selected as the most practical approach during this Phase I system level study. It is anticipated that additional system reliability improvement can be achieved at the circuit level, by use of selected piece part redundancy, during a Phase II detail design activity. The Earth-Mars mode switch, for example, is an obvious candidate for piece part redundancy. Further discussion of piece part redundancy is included in Section 5.2.9.2.

4.5 DISTRIBUTION

An important distinction between flyby and orbiter missions concerns the time criticality of providing power for science loads. In a flyby mission there is a limited time period associated with planetary science data acquisition, while in an orbiter mission, of course, this period is extended many times.

This difference influences the means of power distribution to these science loads. In the flyby case, it is generally adequate to consider a minimum number of power control switches for the science loads, since they are required to operate more or less simultaneously. In the orbiter case, it is possible to consider that the science loads need not operate simultaneously in which case separate power control switches would be used.

There are several potential advantages in this approach:

a. Peak demands could be reduced avoiding possible dependence on battery power. Although the solar array power appears adequate for simultaneous science load operation (see Section 4.6), the situation appears marginal at increased sun distances. By using separate switches with science load sequencing, it is possible, in effect, to increase the margin of the system and provide increased operational flexibility.

b. The use of separate switching permits the consideration of resettable load fault protection. An approach for accomplishing this is shown on Figure 4.4-1. First, concerning critical engineering loads (A/C, CC&S, FCS, etc.) the use of fault protection is not considered on the basis that any degree of mission success depends on these loads and therefore, fault protection is of no use.

The loss of any single science load, on the other hand, does not imply total mission loss and therefore, fault protection may be appropriate. As shown in Figure 4.4-1, the current associated with these loads passes through an overcurrent sensor. A severe fault in any single noncritical load would cause all of the associated power control relays to trip to their reset positions. Isolation of the specific fault can be achieved by attempting to set each relay individually or possibly through interpretation of the science load telemetry information. Of course, it is possible to employ separate overcurrent trips for each load. The use of the single trip is only suggested as a means of achieving economy when, in fact, the use of several such trips might be more appropriate, especially from a reliability standpoint.

The size of the loads protected by any single overcurrent trip is limited by the overload capability of the main inverter and this will influence the number of trips that should be used. This is described in Section 5.1.5.

As shown on Figure 4.4-1, the reset positions of the science loads introduce substitute heater loads. This reflects the approach used on the MM '69 system. It is presumed that this was done to take convenient advantage of the back contacts of the load control switch, avoiding the need for additional relays and harnesses. Since the suggested overcurrent trip transfers the switches to their reset positions, it is necessary to provide fused fault protection for the heaters as was done on the MM '69 system. As described later in Section 5.1.5.1, the fuse ratings must be selected to prevent overloading of the main inverter. With this constraint, it may be necessary to use several smaller heater elements, each separately fused, in place of a single larger element.

A major drawback to the use of additional science switches is the necessity for additional command capability. The trade studies to assess the potential gain versus cost is essentially a spacecraft system question and beyond the scope of this study.

4.6 PERFORMANCE

4.6.1 SIZING ANALYSIS -- RECOMMENDED SHUNT SYSTEM

The sizing of the system elements is based on the load requirements and mission time factors described in Section 3 and the block diagram in Figures 4.1-1 and 4.4-1. Table 4.6-1 shows the procedure used in determining the power handling requirements for the system equipment. This procedure is reviewed below:

- The mission phases are shown as the column headings of the table.
- Lines 1 and 2 list the time duration associated with battery demand periods only.
- Lines 3, 6, 9 and 14 list the summed totals for the types of distributed power taken from Table 3-1.
- Lines 5, 8 and 11 list power input at the associated inverters using the inverter efficiency data shown on Table 4.6-2.
- Line 12 represents the input to the 400 Hz inverter diode, (F) or (F') in Figure 4.4-1.
- Line 13 is the total regulated bus demand.
- Line 16 is the input to the propulsion system regulated converter which is obtained by dividing the output of line 14 by the efficiency factor of line 15.
- Line 18 lists the boost efficiency data from Table 4.6-2 based on line 13 demand for a battery discharge condition. As shown, boost operation is implied only during battery demand periods. Although the boost regulator may operate during cruise in the Earth-mode switch position, this is not considered in the calculation since it does not represent a power limiting condition.
- Line 19 lists the demand at the boost regulator input.
- Line 20 lists demand at the battery terminals associated with the boost regulator and raw loads. A diode drop allowance of 3 percent is made for the raw loads.
- Line 21 calculates the associated watt-hour demand based on line 1 time durations for the launch, maneuver, orbit insertion and orbit trim phases.
- Line 23 calculates the regulated converter watt-hour demand based on the line 2 engine burn-time durations.

Step No.	Parameter	Computation Procedure	One Launch	Two Star Acquisition	Three Cruise I (Battery Charger On)	Four Cruise II (Battery Charger Off)	Five Maneuver
1	Duration (minutes)		67	-	-	-	84
2	Engire Burn Time (minutes)		-	-	-	-	0.4
3	2.4 kHz Inverter Output (w)		188.95	182.95	161.95	161.95	179.45
4	2.4 kHz Inverter Eff.		0.912	0.911	0.903	0.903	0.910
5	2.4 kHz Inverter Input (w)	(3) ÷ (4)	207.10	200.84	179.35	179.35	197.18
6	400 Hz, 3Φ Inverter Output (w)		9.00	9.00	9.00	9.00	9.00
7	400 Hz, 3Φ Inverter Eff.		0.775	0.775	0.775	0.775	0.775
8	400 Hz, 3Φ Inverter Input (w)	(6) ÷ (7)	11.61	11.61	11.61	11.61	11.61
9	400 Hz, 1Φ Inverter Output (w)		-	-	-	-	-
10	400 Hz, 1Φ Inverter Eff.		-	-	-	-	-
11	400 Hz, 1Φ Inverter Input (w)	(9) ÷ (10)	-	-	-	-	-
12	400 Hz, Inverter Diode Input (w)	((8) + (11)) 56/55	11.8	11.8	11.8	11.8	11.8
13	Reg Bus Demand (w)	(5) + (12)	218.9	212.6	191.2	191.2	209.0
14	Propulsion Converter Output (w)		-	-	-	-	65.0
15	Propulsion Converter Efficiency		-	-	-	-	0.870
16	Propulsion Converter Input (w)	(14) ÷ (15)	-	-	-	-	74.71
17	Raw Demand (w)		68.7	68.7	81.5	81.5	68.7
18	Boost Efficiency		0.842	-	-	-	0.842
19	Boost Input (w)	(13) ÷ (18)	269.0	-	-	-	248.0
20	Battery Demand - Raw + Boost Input (w)	(17) ÷ .97 + (19)	331.0	-	-	-	319.0
21	Watt-Hrs Out - Raw + Boost Input (w-Hr)	((20) x (1)) ÷ 60	370.0	-	-	-	446.0
22	Battery Demand - Reg Conv. (w)	(16)	-	-	-	-	74.7
23	Watt-Hrs Out - Reg Conv. (w-Hr)	((22) x (2)) ÷ 60	-	-	-	-	0.5
24	*Power System Losses - Raw + Boost (w-Hr)	(Power loss) x (1) 60	5.0	-	-	-	6.3
25	*Power System Losses - Reg Conv. (w-Hr)	(Power loss) x (2) 60	-	-	-	-	0.014
26	Total Watt-Hrs Out (w-Hr)	(25) + (24) + (23) + (21)	375.0	-	-	-	453.0
27	Req'd. Watt-Hrs In (w-Hr)	(26) x 1.77	664.0			-	802.0
28	Recharge Time (Hr)		-	-	14.0	-	-
29	Charge Power (w)	(27) ÷ (28)	-	-	47.4	-	-
30	Charger Input (w)	(29) x 38.3/35	-	-	51.9	-	-
31	Total Raw Output (w)	(30) + (17) + 38.3/37.5 (13)	-	286.0	329.0	277.0	-
32	*Power System Losses (w)		-	10.0	11.0	10.0	-
33	Array Demand (w)	((31) + (32)) 39./38.3	-	302.0	346.0	292.0	-

*Power System Losses

	Boost Operation	Shunt Operation
Line Losses	1%	1%
Fault Sensor Losses	0.8 w	0.8 w
Boost Standby Losses	-	6.0 w
Shunt and Standby Losses	0.5 w	0.5 w
Total	1.3 w + 1%	7.3 w + 1%

FOLDOUT [redacted]

Table 4.6-1. Shunt System

Six Far Encounter	Seven Orbit Insertion	Eight Playback-Far Encounter		Nine Orbit Trim		Ten Orbit Cruise CC&S Update		Eleven TV Sequence		Twelve Earth Occultation		Thirteen Playback ATR		Fourteen Playback DTR	
-	96	-		84.0		-		60.0		-		162.0		24.0	
-	13	-		1.0		-		-		-		-		-	
214.15	179.45	170.95		179.45		161.95		207.15		166.95		170.95		169.95	
0.918	0.910	0.907		0.910		0.903		0.917		0.905		0.907		0.907	
233.18	197.18	188.47		197.18		179.35		225.97		184.45		188.47		187.46	
9.00	9.00	9.00		9.00		9.00		9.00		9.00		9.00		9.00	
0.775	0.775	0.775		0.775		0.775		0.775		0.775		0.775		0.775	
11.61	11.61	11.61		11.61		11.61		11.61		11.61		11.61		11.61	
12.00	-	-		-		-		15.50		-		-		-	
0.820	-	-		-		-		0.838		-		-		-	
14.63	-	-		-		-		18.50		-		-		-	
26.7	11.8	11.8		11.8		11.8		30.7		11.8		11.8		11.8	
259.9	209.0	200.3		209.0		191.2		256.7		196.3		200.3		199.3	
-	65.0	-		65.0		-		-		-		-		-	
-	0.870	-		0.870		-		-		-		-		-	
-	74.71	-		74.71		-		-		-		-		-	
115.5	102.7	102.7		68.7		68.7		102.7		81.5		115.5		81.5	
-	0.842	-		0.842		-		-		-		-		-	
-	248.0	-		248.0		-		-		-		-		-	
-	354.0	-		319.0		-		-		-		-		-	
-	566.0	-		446.0		-		-		-		-		-	
-	74.7	-		74.7		-		-		-		-		-	
-	16.2	-		1.2		-		-		-		-		-	
-	7.8	-		6.3		-		-		-		-		-	
-	0.4	-		0.03		-		-		-		-		-	
-	590.0	-		453.0		-		-		-		-		-	
-	1043.0			801.0											
-	-	-	22.0	-	-	18.5		-	-	18.5		-	21.0	-	18.5
-	-	-	47.5	-	-	43.3		-	-	43.3		-	38.2	-	43.3
-	-	-	52.0	-	-	47.4		-	-	47.4		-	41.8	-	47.4
381.0	-	308.0	360.0	-	263	311.0		365.0	282	329		321	362.0	285	332.0
11.0	-	10.0	11.0	-	10.	10.0		11.0	10	11		10	11.0	10	11.0
400.0	-	324.0	378.0	-	278	327.0		382.0	297	346		337	380.0	300	350.0

FOLDOUT FRAME 2

Table 4.6-2. Power Subsystem Output and Efficiency Data

PW1	12.50	25.00	37.50	50.00	62.50	75.00	87.50	100.00	112.50	125.00
EF1	0.560	0.660	0.710	0.745	0.775	0.805	0.833	0.853	0.867	0.877
PW1	137.50	150.00	162.50	175.00	187.50	200.00				
EF1	0.887	0.903	0.903	0.909	0.912	0.915				
PW2	4.00	5.00	6.00	7.00	8.00	9.00	10.00	11.00	12.00	13.00
EF2	0.650	0.680	0.710	0.738	0.758	0.775	0.790	0.800	0.810	0.820
PW2	14.00	15.00	16.00	17.00	18.00	20.00				
EF2	0.828	0.835	0.840	0.846	0.850	0.860				
PW3	4.00	5.00	6.00	7.00	8.00	9.00	10.00	11.00	12.00	13.00
EF3	0.650	0.695	0.730	0.760	0.780	0.793	0.804	0.814	0.820	0.827
PW3	14.00	15.00	16.00	17.00	18.00	20.00				
EF3	0.831	0.836	0.840	0.843	0.848	0.850				
PW4	20.00	35.00	50.00	60.00	75.00	85.00	95.00	105.00	115.00	125.00
EF4	0.585	0.670	0.758	0.775	0.797	0.809	0.819	0.828	0.833	0.837
PW4	135.00	150.00	175.00	200.00	225.00	250.00				
EF4	0.840	0.842	0.842	0.842	0.842	0.838				
PW5	20.00	35.00	50.00	60.00	75.00	85.00	95.00	105.00	115.00	125.00
EF5	0.600	0.680	0.765	0.782	0.803	0.817	0.835	0.840	0.848	0.857
PW5	135.00	150.00	175.00	200.00	225.00	250.00				
EF5	0.863	0.870	0.876	0.880	0.880	0.880				
PW6	20.00	35.00	50.00	60.00	75.00	85.00	95.00	105.00	115.00	125.00
EF6	0.620	0.700	0.773	0.788	0.810	0.825	0.838	0.848	0.857	0.865
PW6	135.00	150.00	175.00	200.00	225.00	250.00				
EF6	0.870	0.876	0.883	0.887	0.887	0.887				
PW7	20.00	35.00	50.00	60.00	75.00	85.00	95.00	105.00	115.00	125.00
EF7	0.870	0.870	0.870	0.870	0.870	0.870	0.870	0.870	0.870	0.870
PW7	135.00	150.00	175.00	200.00	225.00	250.00				
EF7	0.870	0.870	0.870	0.870	0.870	0.870				
EFL	0.970									

Power Subsystem Notation

One	=	Main inverter (2.4 kHz)
Two	=	Attitude control inverter (400 Hz, 3ϕ)
Three	=	Single phase inverter (400 Hz)
Four	=	Booster regulator - battery
Five	=	Booster regulator - solar power - near Earth
Six	=	Booster regulator - solar power - near Mars
Seven	=	Regulated converter (28 vdc)

- Lines 24 and 25 calculate the power system losses in watt-hours for the raw and boost regulator input and for the regulated converter. The power loss allowances, as summarized at the bottom of the table, include a 1 percent loss in the power system harnessing plus the fixed losses associated with the fault sensor, boost standby and shunt amplifier standby. Note that the boost standby loss does not apply when the boost regulator is operating (e.g., during battery discharge).

- Line 26 is the total watt-hour demand including all losses.

- Line 27 lists the battery recharge watt-hours relative to the discharge watt-hours of line 26. The 1.77 factor is based on a relative charge to discharge voltage ratio of 1.94/1.45 and a 32 percent excess current capability to take account of ampere-hour efficiency and current tapering near the end of the recharge cycle. Thus,

$$\frac{1.94}{1.45} \times 1.32 = 1.77$$

- Ignore lines 28, 29 and 30 for the moment and consider array power requirements without battery recharge power. This is shown on the left subdivision of the columns below line 27 for the mission phases associated with solar array operation.

- Line 31 indicates required output at the raw array bus which includes the raw demand (item 17) plus regulated demand (item 13) with allowance for loss through the main in-line diode.

- Line 33 lists the net array output requirements accounting for the power system losses of line 32. This is the power requirement reflected to the array side of the isolation diode. As indicated, the highest demand not including battery recharge is 382 watts associated with the TV sequence phase. This value establishes the minimum array power requirement assuming the battery is not used to satisfy this peak load condition. This is a desirable objective in that battery cycling is avoided. The problem now is to determine how much additional array power, if any, is required to satisfy battery recharge.

- Returning then to line 28, refer first to the "Playback Far Encounter" mission phase. The study guidelines indicate that at least 24 hours will elapse before an Orbit Trim maneuver is initiated subsequent to Orbit Insertion. It is assumed that the acquisition of science data will be highly desirable during this period. This pertains to the "TV Sequence" phase which will occur over an estimated period of one hour during periapsis passage. Two such sequences will occur during the first 24 hours assuming insertion into a 12-hour Earth synchronous orbit. Thus, with no battery recharging during the TV sequences only 22 recharge hours are available as shown on line 28.

Proceeding down the right-hand subdivision of the "Playback Far Encounter" phase:

- Line 29 identifies charge power at the battery input terminals.

- Line 30 takes account of charge regulator losses. Since a series dissipative regulator is used, the ratio of power input to output is identical to the input/output voltage ratio. The 35-volt output corresponds to the battery charging voltage for the 18 cell battery using 1.04 volts/cell. The 38.3-volt input makes allowance for the main in-line diode (A), Figure 4.1-1 or 4.4-1, drop to the regulated bus at the boost regulator output.

- Lines 31 and 33 are as described previously with allowance made for the charge power.

The indicated array power requirement for the "Playback Far Encounter" phase is 378 watts and, therefore, no additional array capability is required over that determined for the "TV Sequence."

The "Playback Far Encounter" phase is the only one assumed to occur between Orbit Insertion and the first Orbit Trim. Other lower power modes may occur during this period and advantage may be taken of the additionally available charging power. The 47.5-watt recharge rate corresponds to a current of 1.4 amperes. For the 50 ampere-hour silver-zinc cells used, it is safe to use a 2-ampere charging rate and thereby achieve a more rapid recharge. This is the level to which the charge regulator would be set. The preferential inhibit of charge power in the shunt system discussed previously makes this possible without incurring performance penalties.

Using the required 1.4-ampere rate (as distinguished from the 2-ampere setting) on the charge regulator, it is now possible to examine its effect during other mission phases. First, subsequent to launch, a 14-hour period is required for recharging as shown on line 28 for the "Cruise" phase. Charging periods are also checked for the mission phases beyond "Orbit Trim." These cases are checked to assure that recharging can be accomplished within a 22-hour span with the same criterion in mind as between Orbit Insertion and Orbit Trim discussed earlier. In this instance, the criterion is that two Orbit Trim maneuvers could occur no closer than 24 hours apart. Again, allowance is made for two, 1-hour TV sequences. As shown, none of the recharge times exceed 22 hours and therefore the 1.4-ampere rate is adequate. Note that it was necessary to reduce this rate slightly during the "Playback ATR" phase in order that the 382-watt array power requirement cannot be

exceeded, but even in this case sufficient recharge time is available. Again the charge power is preferentially reduced in response to limited solar array capability. The "Playback ATR" calculation shows that its higher power level could exist during the entire 22-hour period, although, in fact, it will only last about 2.4 hours.

4.6.2 SIZING ANALYSIS -- MM '69 POWER SYSTEM APPLIED TO THE MARS ORBITER PROFILE

Table 4.6-3 shows system sizing calculations adapting the MM '69 system to the Mars '71 load profile. This is done as a means of comparison with the recommended shunt system.

The calculation procedures are similar to those described for the shunt system with minor differences as noted on the table.

The key items affecting solar array sizing for the two systems occur at phase no. 11, "TV Sequence." The MM '69 system requires 410 watts and the shunt system requires 382 watts. Hence, for an identical solar array for both systems the more efficient shunt system would provide an additional 28 watts which is approximately a 7 percent gain in useful power.

4.6.3 PERFORMANCE COMPARISON OF MM '69 AND SHUNT SYSTEMS

4.6.3.1 Solar Array Margin Comparison

In a shunt regulated system, power is taken from the solar array at a fixed voltage level. To examine the sensitivity of available array power at fixed voltages to array performance uncertainties, two extreme cases of voltage-current prediction were examined. Both considered the use of the MM '69 solar panel design.

Case I

The assumed conditions used in this V-I prediction are listed in Table 4.6-4. The resulting P-V curves are shown in Figure 4.6-1 and were generated with the aid of a solar array prediction computer program which is briefly described in Section 4.6.3.2. The related temperature profile is shown on Figure 4.6-2 and is based on thermal radiation energy balance considerations using a starting temperature of 60°C at 1.0 AU.

Table 4.6-3. MM '69 Boost System

Step No.	Parameter	Computation Procedure	Flight Phase: One Launch	Two Star Acquisition	Three Cruise I (Battery Charger On)	Four Cruise II (Battery Charger Off)	Five Maneuver	Six Far Encounter	Seven Orbit Insertion	Eight Playback Far Encounter	Nine Orbit Trim	Ten Orbit Cruise CC&S Update	Eleven TV Sequence	Twelve Earth Occultation	Thirteen Playback ATR	Fourteen Playback DTR
1	Duration (Minutes)		67				84		96		84		60		162	74
2	Engine Burn Time (Minutes)						0.4		13		1					
3	24 kHz Inverter Output (W)		188.95	182.95	161.95	161.95	179.45	214.15	179.45	170.95	179.45	161.95	207.15	196.95	170.95	169.95
4	24 kHz Inverter Efficiency		0.912	0.911	0.903	0.903	0.910	0.918	0.910	0.907	0.910	0.903	0.917	0.905	0.907	0.907
5	24 kHz Inverter Input (W)	③ ÷ ④	207.10	200.84	179.35	179.35	197.18	233.18	197.18	188.47	197.	179.35	225.97	184.45	188.47	187.46
6	400 Hz, 3Ø Inverter Output (W)		9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00
7	400 Hz, 3Ø Inverter Efficiency		0.775	0.775	0.775	0.775	0.775	0.775	0.775	0.775	0.775	0.775	0.775	0.775	0.775	0.775
8	400 Hz, 3Ø Inverter Input (W)	⑥ ÷ ⑦	11.61	11.61	11.61	11.61	11.61	11.61	11.61	11.61	11.61	11.61	11.61	11.61	11.61	11.61
9	400 Hz, 1Ø Inverter Output (W)							12.00					15.50			
10	400 Hz, 1Ø Inverter Efficiency							0.820					0.838			
11	400 Hz, 1Ø Inverter Input (W)	⑨ ÷ ⑩						14.63					18.50			
12	400 Hz Inverter Diode Input (W)	⑤ + ⑪ 56/55	11.8	11.8	11.8	11.8	11.8	26.7	11.8	11.8	11.8	11.8	30.7	11.8	11.8	11.8
13	Reg. Bus Demand (W)	⑤ + ⑫	218.9	212.6	191.2	191.2	209.0	259.9	209.0	200.3	209.0	191.2	256.7	196.3	200.3	199.3
14	Propulsion Converter Output (W)						65.0		65.0		65.0					
15	Propulsion Converter Efficiency						0.870		0.870		0.870					
16	Propulsion Converter Input (W)	⑭ ÷ ⑮					74.71		74.71		74.71					
17	Raw Demand (W)		68.7	81.5	81.5	81.5	68.7	115.5	102.7	102.7	68.7	68.7	102.7	81.5	115.5	81.5
18	Boost Efficiency		0.842	0.880	0.879	0.879	0.842	0.887	0.842	0.887	0.842	0.886	0.887	0.886	0.887	0.887
19	Boost Input (W)	⑰ ÷ ⑱	260	241	218	218	248	293	248	225	248	216	289	221	226	225
20	Battery Demand-Raw + Boost Input (W)	(⑰ + ⑲) ÷ .97	339				377		362		327					
21	Watt-Hrs Out-Raw + Boost Input (W-Hr)	(⑳ + ①) ÷ 60	379				458		580		458					
22	Battery Demand-Reg Conv. (W)	⑯ ÷ .97					77		77		77					
23	Watt-Hr Out-Reg Conv. (W-Hr)	(㉒ × ㉓) ÷ 60					0.5		16.7		1.3					
24	Total Watt-Hr Out (W Hr)	(㉑ + ㉔) ÷ .98	387				468		610		469					
25	Req'd Watt-Hr In (W-Hr)	㉕ x 1.77	685				829		1080		830					
26	Recharge Time (Hr)				14					22		16.9		26.9	19.0	15.9
27	Charge Power (W)	㉖ ÷ ㉗			49.0					49.2		49.2		49.2	43.8	49.2
28	Charger Input (W)	㉗ x 38/35			53.2					53.4		53.4		53.4	47.6	53.4
29	Total Raw Output (W)	㉘ + ⑲ + ⑰		323	353	300		409		328 381		285	338	392	303 356	389 307 360
30	Power System Losses (W)	.02 x ㉙		6	7	6		8		6 8		6	7	8	6 7	8 6 7
31	Array-Demand (W)	(㉙ + ㉚) 39/38		338	370	314		417		343 299		298	354	410	317 373	358 408 321 357

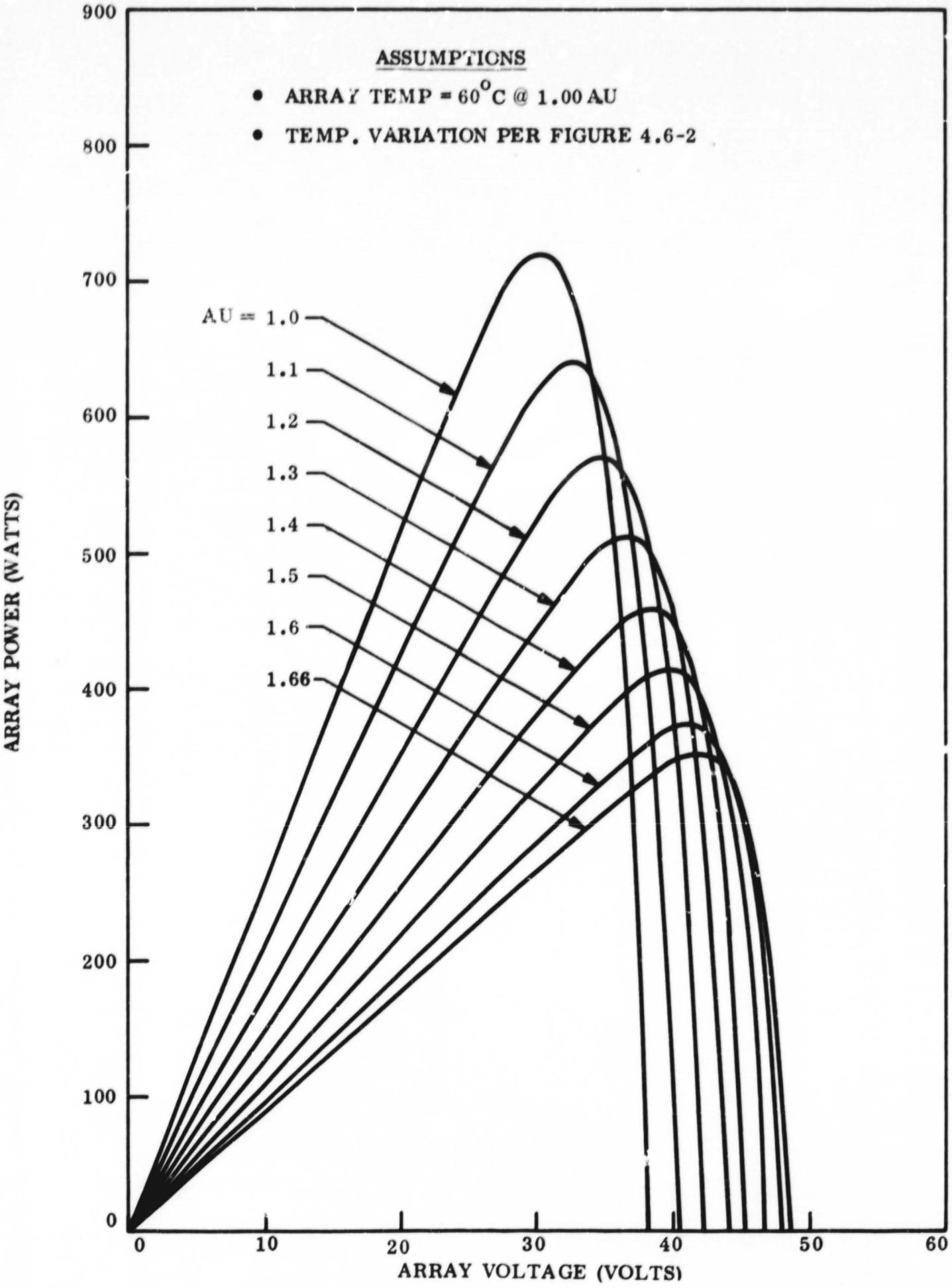


Figure 4.6-1. Predicted Mariner '69 Solar Array P-V Curves

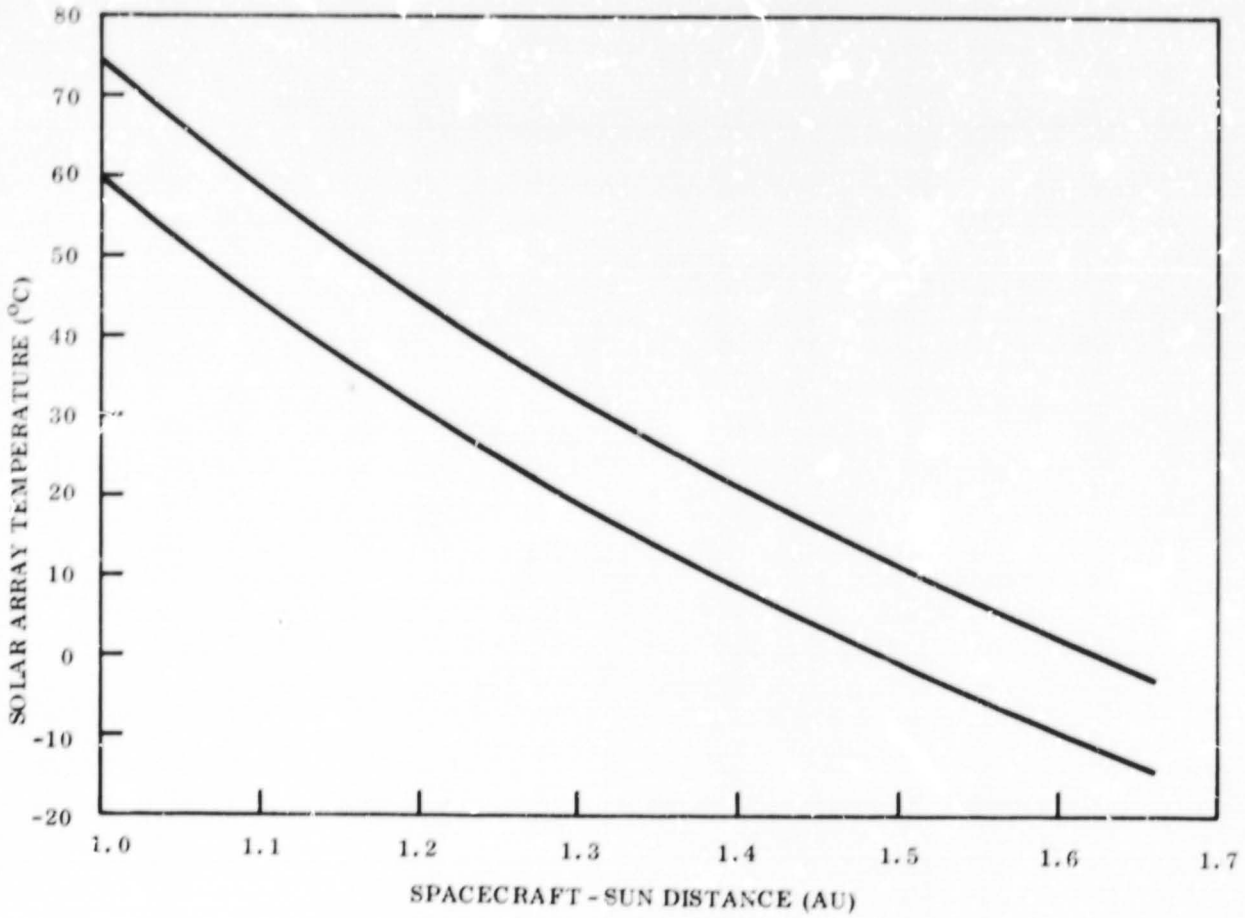


Figure 4.6-2. Solar Array Temperature Versus Sun Distance for Two Different Temperatures at 1.0 AU

Case II

The assumed conditions for this case are also shown in Table 4.6-4. The significant difference is the higher value of temperature at 1.0 AU. The conservatism associated with using this higher temperature (15°C increase) is considered sufficient to permit removal of estimated short-circuit current degradations. The resulting P-V curves are shown on Figure 4.6-3 and the associated temperature profile on Figure 4.6-2.

The two results represent different approaches in accounting for performance uncertainties. Although disagreements may exist on the absolute values of temperatures and degradations used, it is more the intent here to explore the power/voltage sensitivity for extreme conditions.

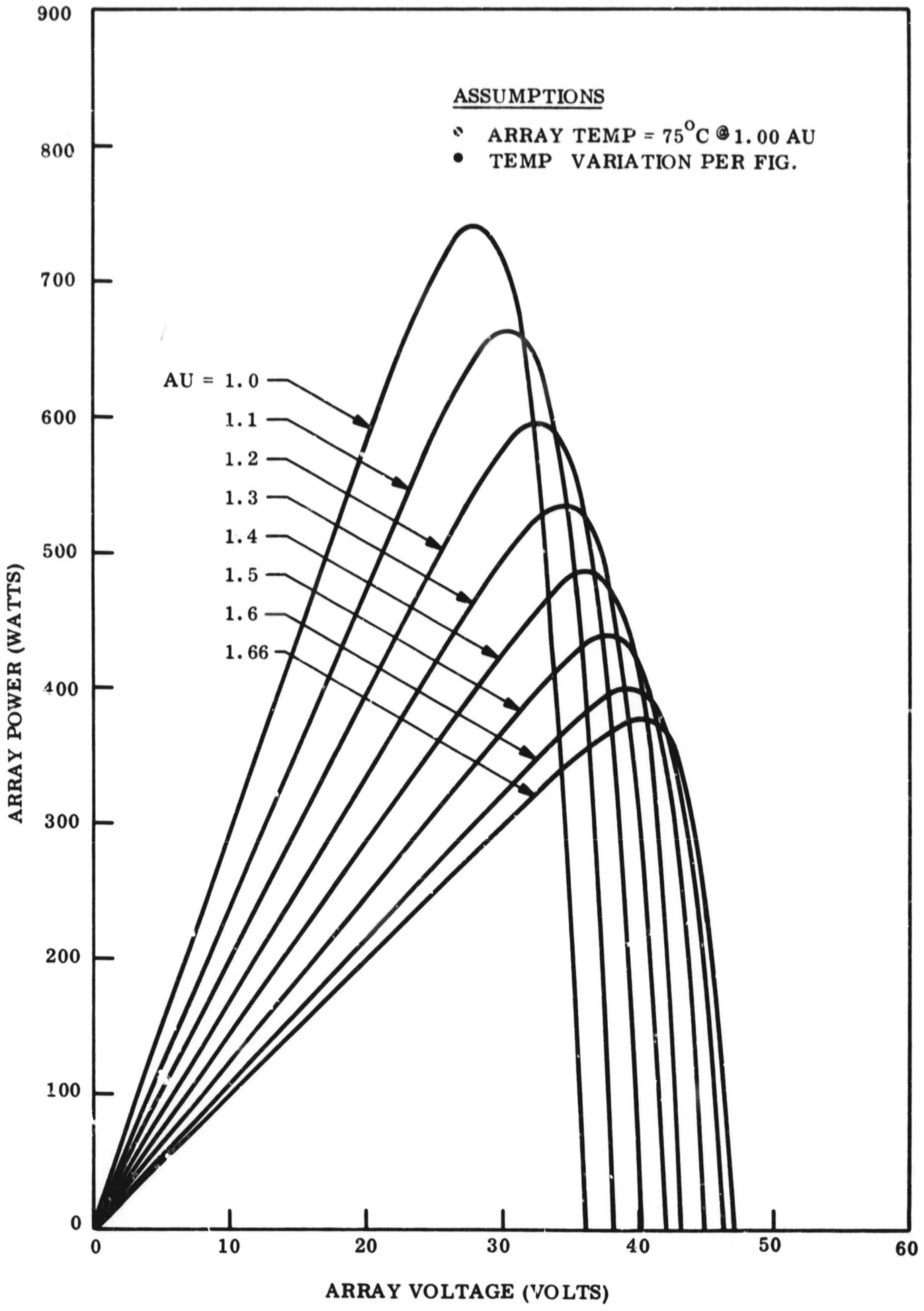


Figure 4.6-3. Predicted Mariner '69 Solar Array P- V Curves

Table 4.6-4. Assumed Conditions for Array Performance Analysis

	Case I	Case II
Array Temperature at 1.0 AU	60^{o}C	75^{o}C
*Radiation Damage Short-Circuit Current Loss Factor $I_{sc}/(I_{sc})_o$	0.966	0.966
Short-Circuit Current Loss Factor due to Misc. Losses and Uncertainties	0.90	1.00
Total Short-Circuit Current Loss Factor	0.870	0.966
*Radiation Damage Open-Circuit Voltage Loss Factor $V_{oc}/(V_{oc})_o$	0.982	0.982

*20-mil cover glass after 9-months, based on the data contained in Section VOY-D-340, Appendix A of the Voyager Task D Final Report, DIN 67SD4379, 16 October 1967, performed for the Marshall Space Flight Center under MSFC Contract No. NAS8-22603.

Plots of the two cases are shown on Figures 4.6-4 and 4.6-5 in terms of power margin for the shunt regulated system and the MM '69 power system. These margins are based on the maximum array demands computed on Tables 4.6-1 [illegible] 4.6-3: 382 watts for the shunt system and 410 watts for the MM '69 system*. The margins for the MM '69 boost system are independent of the array voltage since the boost regulator efficiency is relatively unaffected in the voltage range shown.

The lower demand of the shunt system results in greater margins, though over the limited voltage ranges. To determine the most suitable voltage, cross plots of these margin curves are shown in Figures 4.6-6 and 4.6-7 for each solar array prediction case. Considering the case I cross plot, it is apparent that operation at 40.5 volts would provide power out to the greatest sun distance at 1.58 AU. However, by cross checking this voltage for the case II cross plot, it is seen that marginal performance would occur at 1.4 AU. By backing off to

*Although there are higher loads, they occur at smaller AU distances and are not the critical sizing loads.

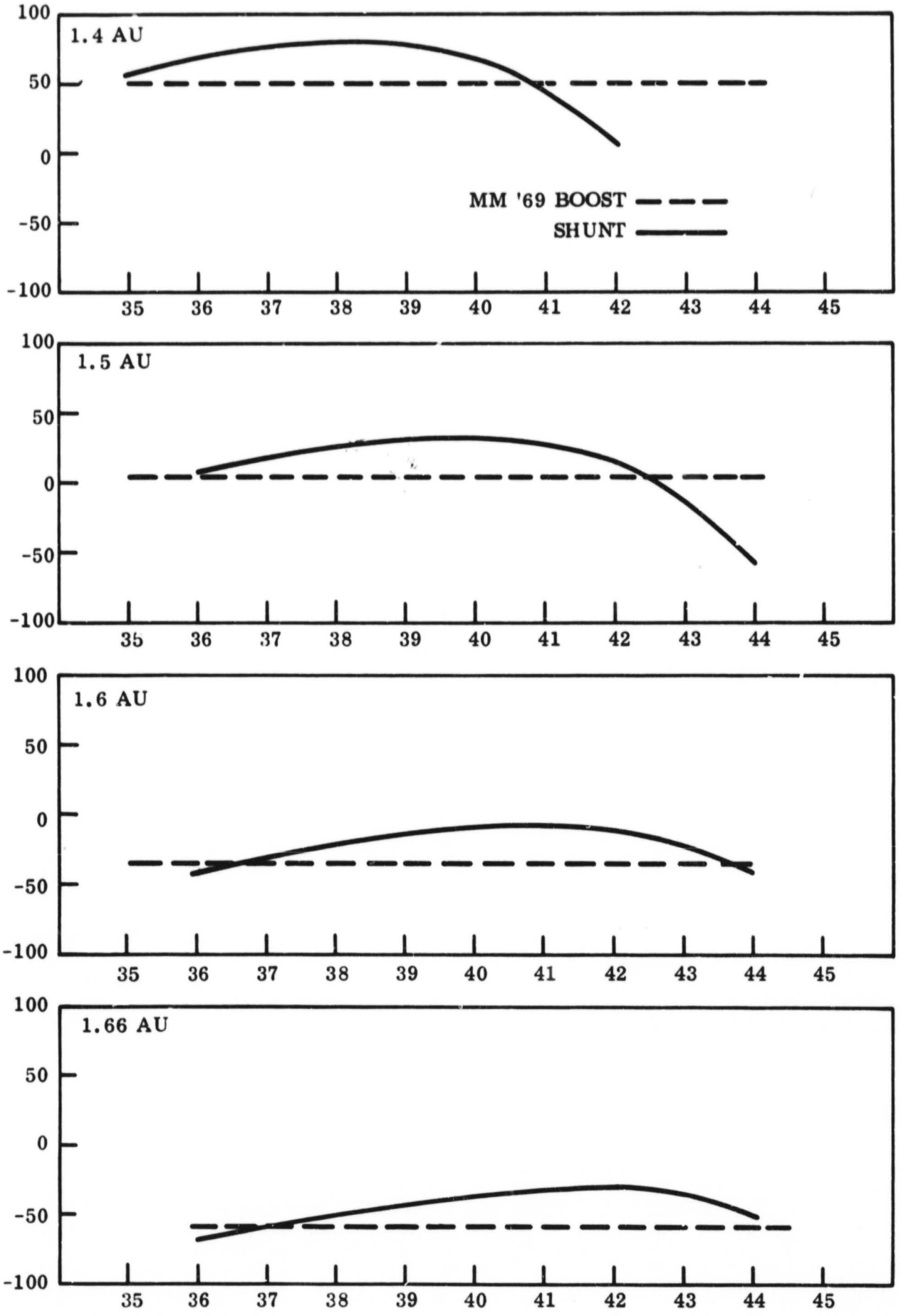


Figure 4.6-4. Array Margin Versus Voltage

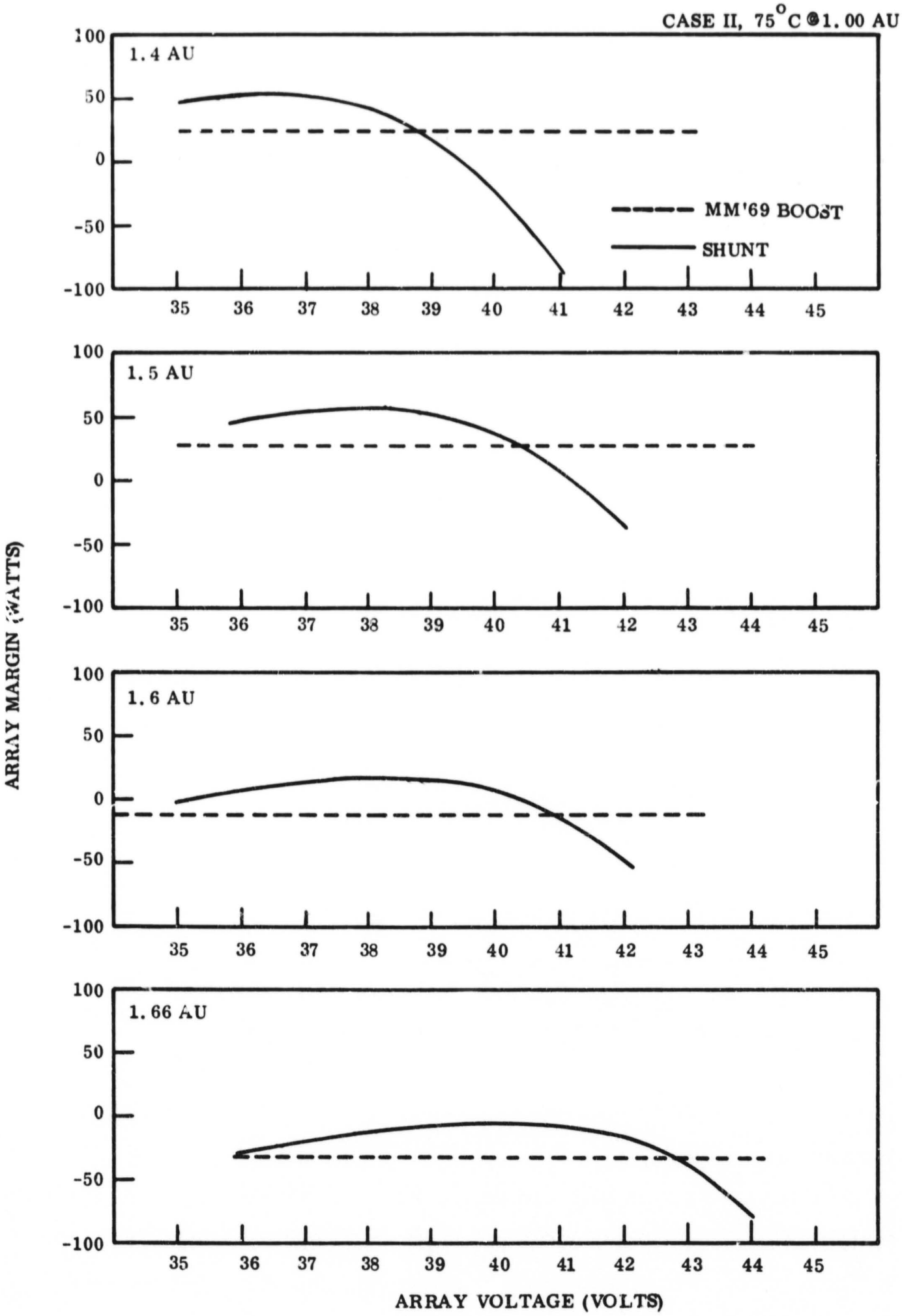


Figure 4.6-5. Array Margin Versus Voltage

39.0 volts, this condition is avoided with only a slight penalty in the maximum AU capability. At this voltage, the shunt system has a margin of about 30 watts at the AU values at which the boost system margin is zero; 1.51 AU for case I and 1.575 AU for Case II.

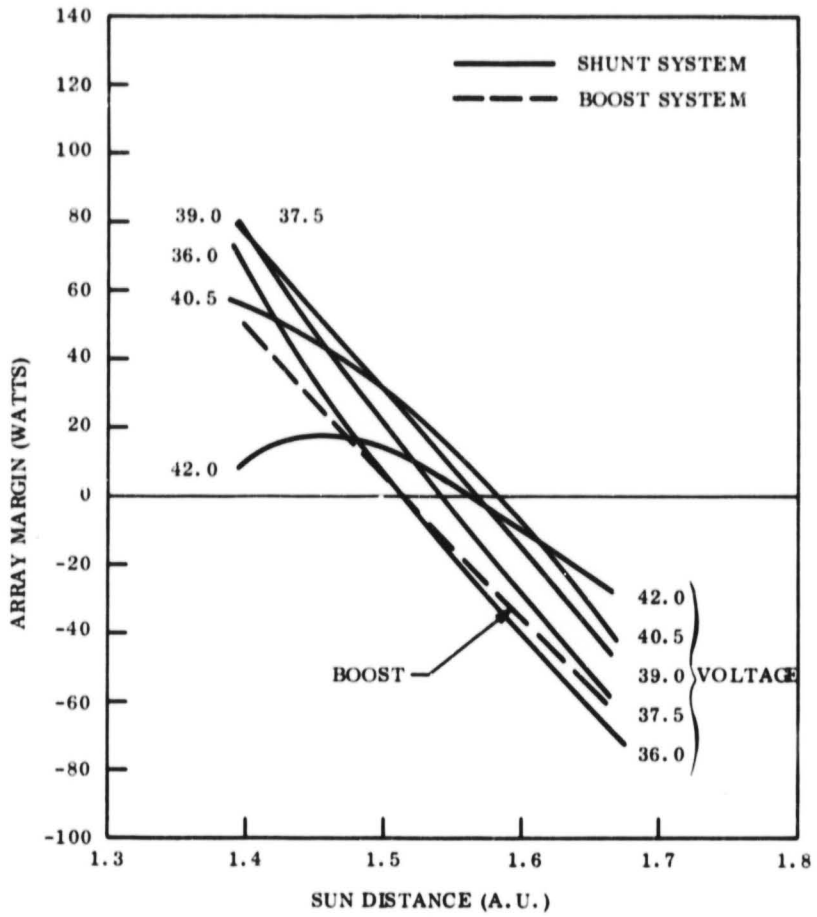


Figure 4.6-6. Case I - Shunt and Boost System Array Margin

On the above basis, 39 volts was selected as the array operating voltage. By examining the cross plot curves, it is seen that voltages down to 37 volts would provide margin. On the high side, 40 to 40.5 volts is the limit considering the penalty at 1.4 AU for case II.

For the orbiter mission, orbit operations are expected to last for 90 days after encounter. For estimated arrival dates in 1971, operation could continue to a sun distance of 1.58 AU as shown on Figure 4.6-8. As shown in the array margin plots, zero margin occurs at 1.57 AU and 1.64 AU for the array prediction models used. It is therefore judged that the shunt system would be adequate for the particular orbiter load profile studied using the MM '69 solar panels.

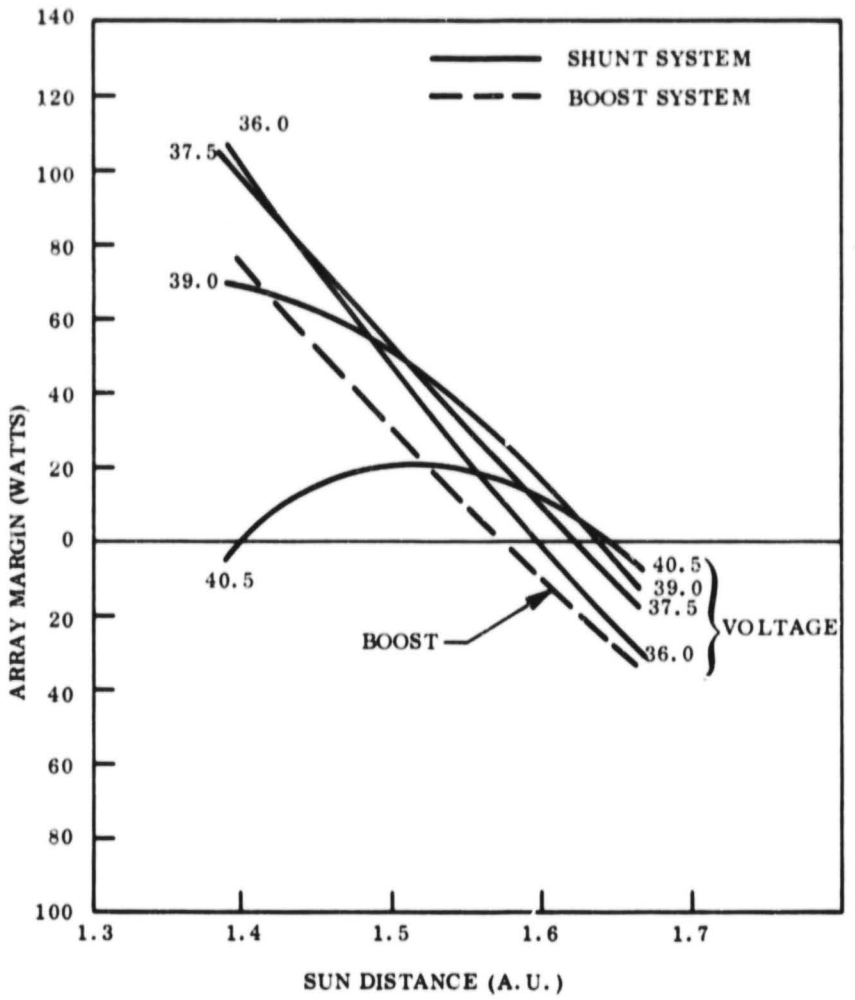


Figure 4.6-7. Case II - Shunt and Boost System Array Margin

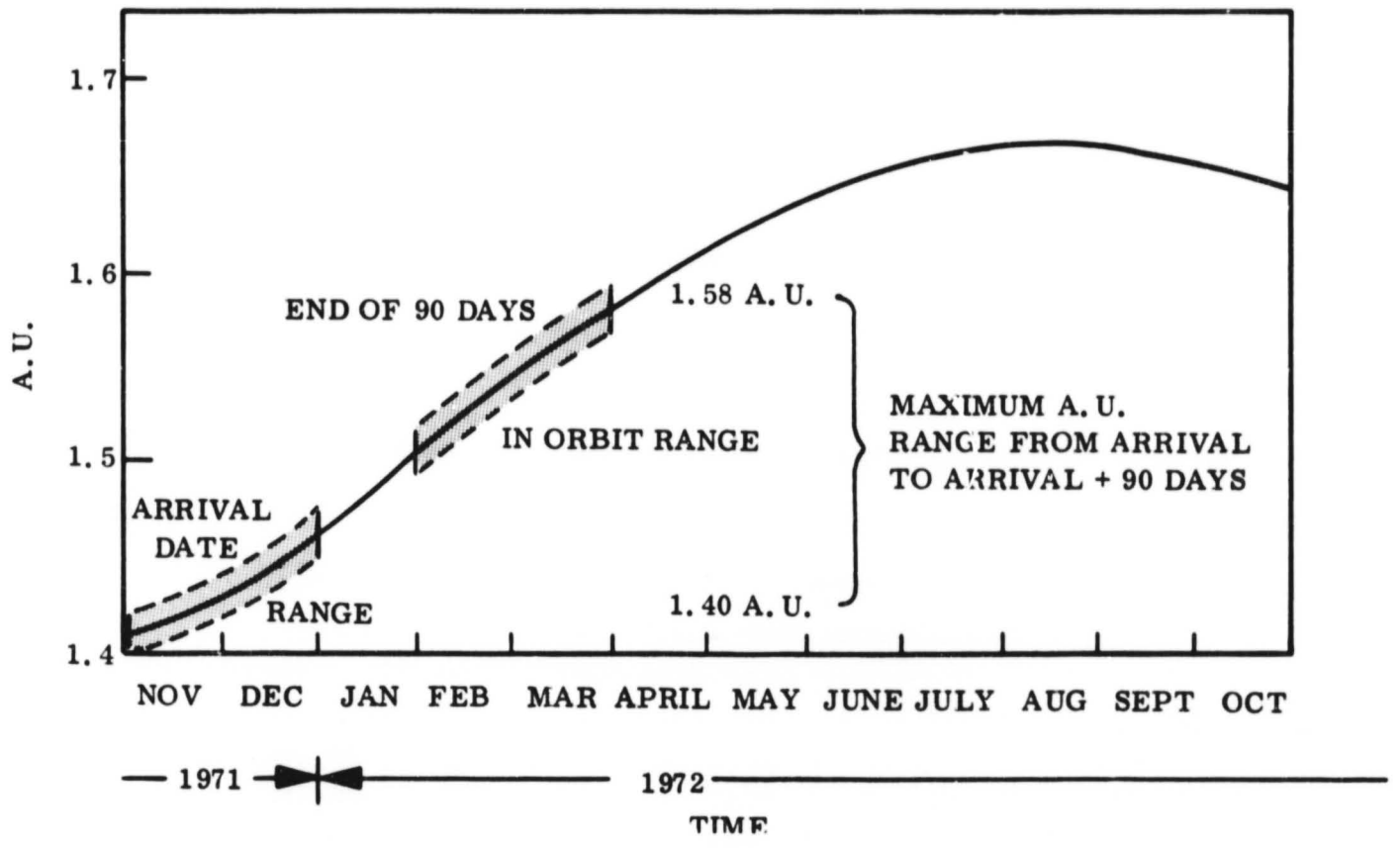


Figure 4.6-8. Typical AU Range for Hypothetical 1971 Mission

4.6.3.2 Other Margin Comparisons

Besides the array power margin discussed earlier, an additional advantage can be identified for the shunt system relative to behavior at array margins of zero or less. With zero margin in the MM '69 system, a slight load instability results in array/battery load sharing. The share boost rectifies this condition momentarily, but the load sharing condition will reoccur if the initial zero margin conditions persist. This undesirable form of system cycling will continue until either the load is reduced or the share boost is inhibited. In the latter situation, power is supplied stably though inefficiently. As noted in an earlier discussion, about 25 percent of the array power may be unavailable in this circumstance and therefore, the battery provides the power deficit.

In contrast, the transition through zero array margin occurs smoothly in the shunt system. No system instability occurs and the full array capability is utilized.

This difference has important ramifications during such periods as the TV sequence phase. For example, assume the array can produce 380 watts as against 382 watts required during a one hour TV sequence pass. The MM '69 system will assume a load sharing mode with the array providing about 286 watts (75% of 380) and the battery providing 96 watts for an energy drain of 96 watt-hours. The shunt system battery will only have to provide about 3 watt-hours allowing for the boost regulator inefficiency and even ignoring the initial higher array margin of the shunt system. In the MM '69 system case additional battery cycling is incurred besides the fact that array recharging power is required.

A related advantage concerns allowable battery charge rates in both the MM '69 and shunt systems. As noted in the sizing calculations, a charge rate of 1.4 amperes is required. A higher setting of 2 amperes is used in the shunt system to permit more rapid recharge when excess array power is available; it is automatically reduced when array power is limited. If this higher limit were used in the MM '69 system under similar array limited circumstances, a sharing mode of operation would result with the associated loss of array power mentioned earlier. Thus, in the MM '69 it is potentially dangerous to use too high a charge rate for reasons of possible system instability. In the shunt system the limit is

dictated more by battery recharge characteristics. Thus, in general, faster recharging is possible with the shunt system. This may have particular significance in the interim recharge period between orbit insertion and orbit trim maneuvers.

4.6.3.3 Array Prediction Technique

The basic data required to predict solar array performance as a function of sun distance are (a) measured voltage-current characteristics (V-I) of solar cells perferably at 1 sun intensity and various temperatures, and (b) temperature-sun distance history. Figure 4.6-9 shows a typical set of voltage-current characteristics at various temperatures for Heliotek, 2 ohm-cm, N/P cells.* Through curve-fitting techniques, these data are stored in a computer program** which can produce the necessary V-I data for any interpolated value of temperature.

The program also produces adjusted V-I curves in response to series and parallel multiplying factors, adjustments in short circuit current, and adjustments in open circuit voltage. Each of these is described below:

a. Series and parallel multiplying factors. This is a straightforward multiplication of current for paralleled cells and voltage for series cells.

b. Short-circuit current adjustment. The short-circuit current at a particular operating temperature and 1 AU is adjusted by a multiplying factor which normally includes the following allowances:

- Filter transmission loss
- Radiation degradation on short-circuit current
- Sun distance $(AU)^{-2}$
- RMS loss and contingency factor which includes:
  - Manufacturing loss
  - Measurement uncertainty
  - Micrometeoroid erosion
  - Ultraviolet effect on filter
  - Random cell failure

*Ralph, E. L., "Performance of Very Thin Silicon Solar Cell," presented at the 6th Photovoltaic Specialist Conference, March 28-31, 1967.

**Computer listings for the GE Time Sharing System were supplied to JPL on this study, although these programs were not developed on the study.

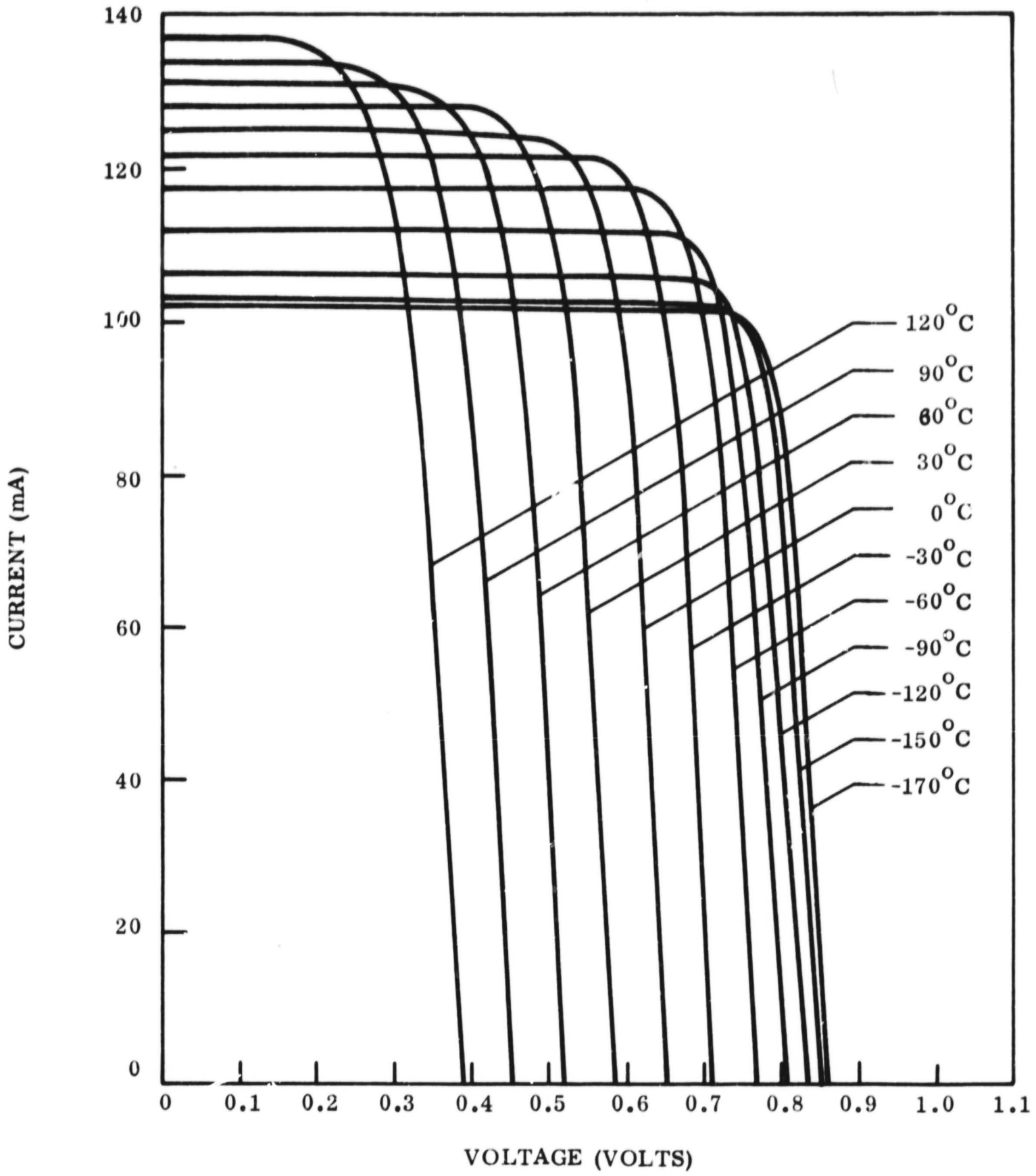


Figure 4.6-9. Voltage-Current Characteristics for Heliotek, 2 ohm-cm, N/P Solar Cell, 3.9 cm^2 active area, 140 mw/cm^2

The predicted V-I characteristic is obtained by translating the 1 AU bare cell characteristic to the adjusted value of short-circuit current. This translation is not purely in the current direction, but also slightly in the voltage direction to take account of a series resistance effect. The method for estimating this effect is shown on Figure 4.6-10. Measurements taken on unilluminated cells show that the diode characteristic shown on the left quadrant has the same basic shape as the illuminated V-I characteristic at 1 AU but is shifted higher in voltage by an amount V_s equivalent to the short-circuit current at 1 AU times R_s the series resistance effect. This effect is temperature sensitive and for the Heliotek cells cited has an average value of about 0.25 ohms. Though the effect is small, the computer program takes it into account by translating the V-I shape along the R_s line to the adjusted value of short-circuit current.

c. Open circuit voltage adjustment. This is a direct translation in the voltage direction to take account of radiation degradation of voltage.

Other features of the program include allowances for protective diode voltage drops and non-normal solar incidence angles.

In applying this program to the MM 69 V-I plots described earlier in Section 4.6.3.1, use was made of experimental results supplied by JPL. These pertain to V-I measurements made on prototype MM '69 panels and associated predictions at various AU distances. The predicted plots are shown on Figure 4.6-11 as solid lines. For each curve, the temperature condition was designated at 15°C lower and the solar intensity at two percent lower than those shown on the figure. This was done as a means for handling uncertainties when, in fact, the V-I plots pertain to the nominal temperature and intensity values shown on the figure.

The approach taken in using the V-I prediction computer program was to first select voltage and current adjustment factors that would duplicate the experimental data as closely as possible. Through several trial and errors, it was found that an open-circuit voltage degradation factor of 0.977 provided a close match as indicated by the points shown in Figure 4.6-11 using the Heliotek cell characteristics cited earlier. No current adjustment factor was necessary. As noted on the plot, matching is excellent at 0.994 and 1.195 AU with a slight shape change for the 1.445 AU case.

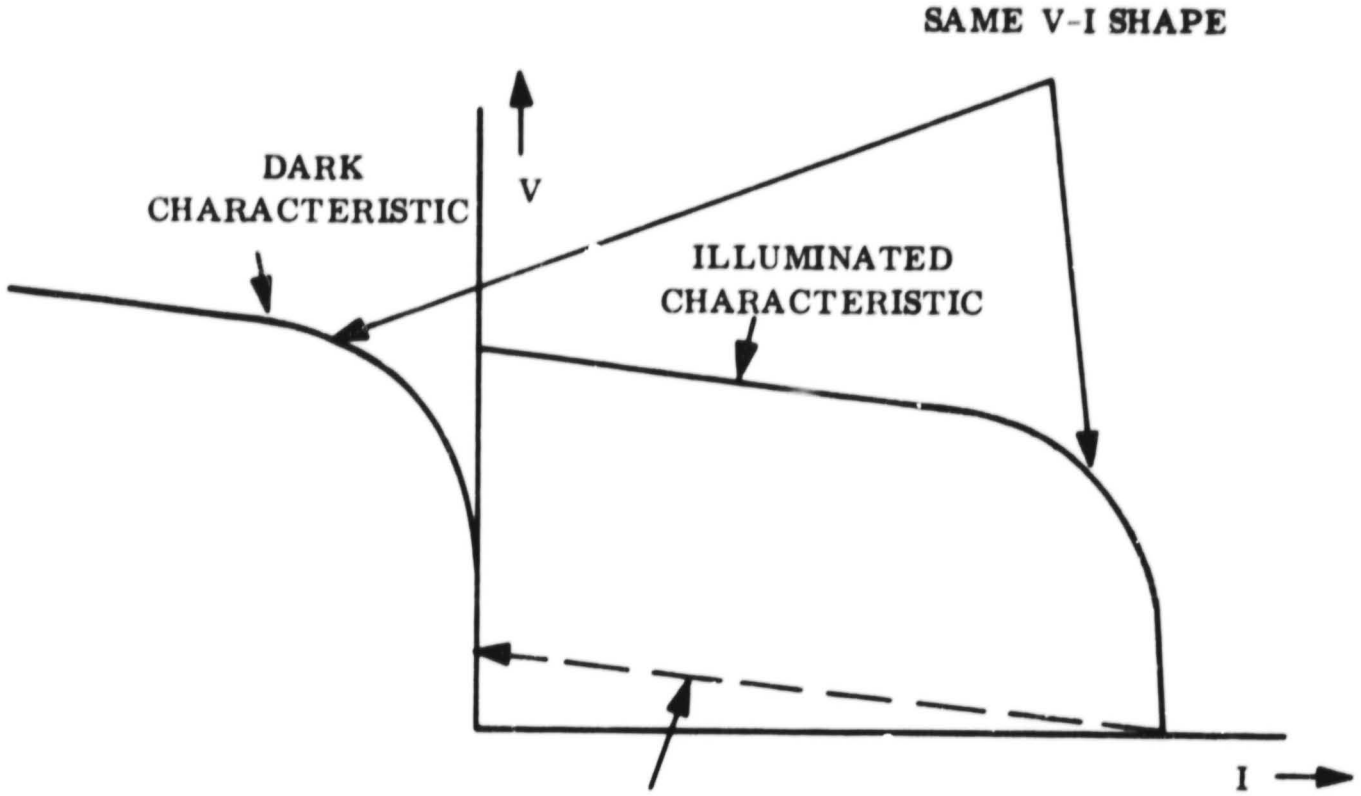


Figure 4.6-10. Voltage-Current Translation for Reduced Illumination

This then served as the basis for nondegraded array performance. Beyond this, expected degradation factors are applied as described for the two cases in Section 4.6.3.1. Since the experimental results take account of filter and cell mismatch losses, no allowance was made for these in the listed degradation of Table 4.6-4.

4.6.4 SHUNT PERFORMANCE

As described in Section 5.1.1, "Baseline Selection," the decision to use a partial shunt regulator was based on reduced thermal dissipation at the shunt elements. Along with the attractiveness of using the MM '69 solar panels it was also desirable to locate the shunt elements on the solar array as a direct substitution for the zener diodes of the MM '69 system. As a feature of failure mode protection, separate shunt elements would be devoted to each of the 24 solar cell sections (6 sections per panel, 4 panels). As pointed out later under Equipment Description, it is quite convenient to wire each shunt element across the first 35 elements of each array section. In terms of the selected array operating voltage (39 volts) discussed earlier, it is then necessary to examine the following limits of performance:

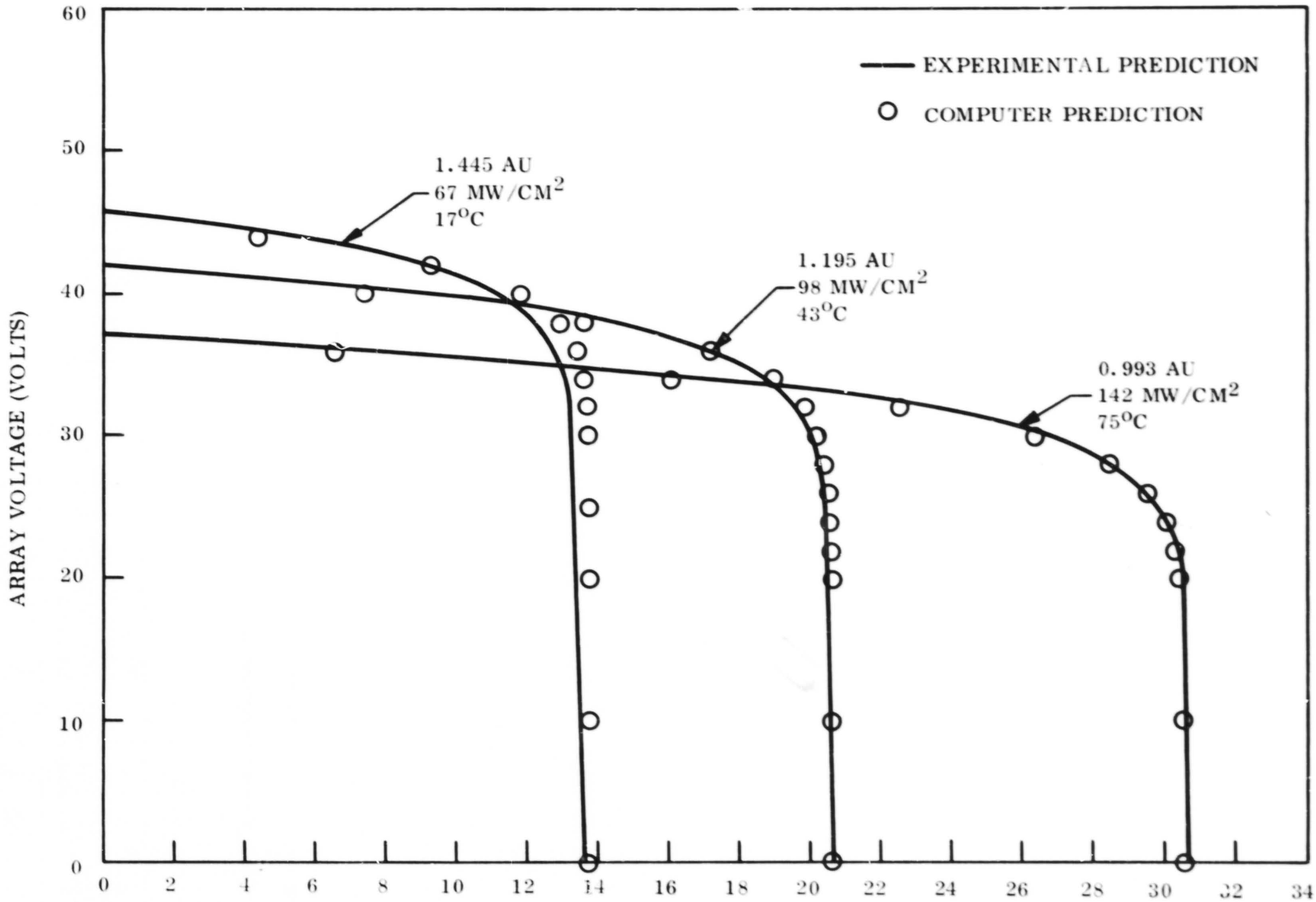


Figure 4.6-11. Reference Mariner '69 V-I Curves

- **Range of array operating conditions for which regulation is maintained.**
- **Maximum value of thermal dissipation and corresponding shunt.**
- **Range of shunt element temperatures.**
- **Allowable number of shunt element failures.**

These questions are considered below.

4.6.4.1 Regulation Limits

With maximum shunting, the voltage available from the shunted array section is equivalent to the minimum drop across the shunt transistor, a value of around one volt. Under this condition, the highest voltage from the upper array section corresponds to its open circuit voltage at zero load conditions. With a regulated dc bus voltage at 37.5 volts, the maximum allowable array voltage is 39 volts (see Figure 4.4-1). Allowing a 1-volt drop across the lower array section, the open circuit voltage for each of the 43 elements in the upper array section is 38/43 = 0.88 volts. Considering the use of solar cells having the characteristics shown on Figure 4.6-9, it is seen that the allowable array temperature is less than -170^{o}C (-274^{o}F). The temperature history curve of Figure 4.6-12 shows a minimum Mars temperature of about 0^{o}F during steady state solar illumination. The decay curve indicates a further temperature decrease if a solar occultation were encountered. Considering an extremely long occultation period, it is seen that the -274^{o}F limit is never reached.

Regulation can therefore be provided by the partial shunt elements wired across the first 35 elements considering worst case temperature and minimum load conditions. At the other extreme where no shunting occurs, regulation depends on array output capability.

4.6.4.2 Thermal Dissipation

In determining the maximum possible shunt dissipation, use was made of a computer program which combines the array prediction technique described in Section 4.6.3.2 with specific shunt parameters. The input parameters used are:

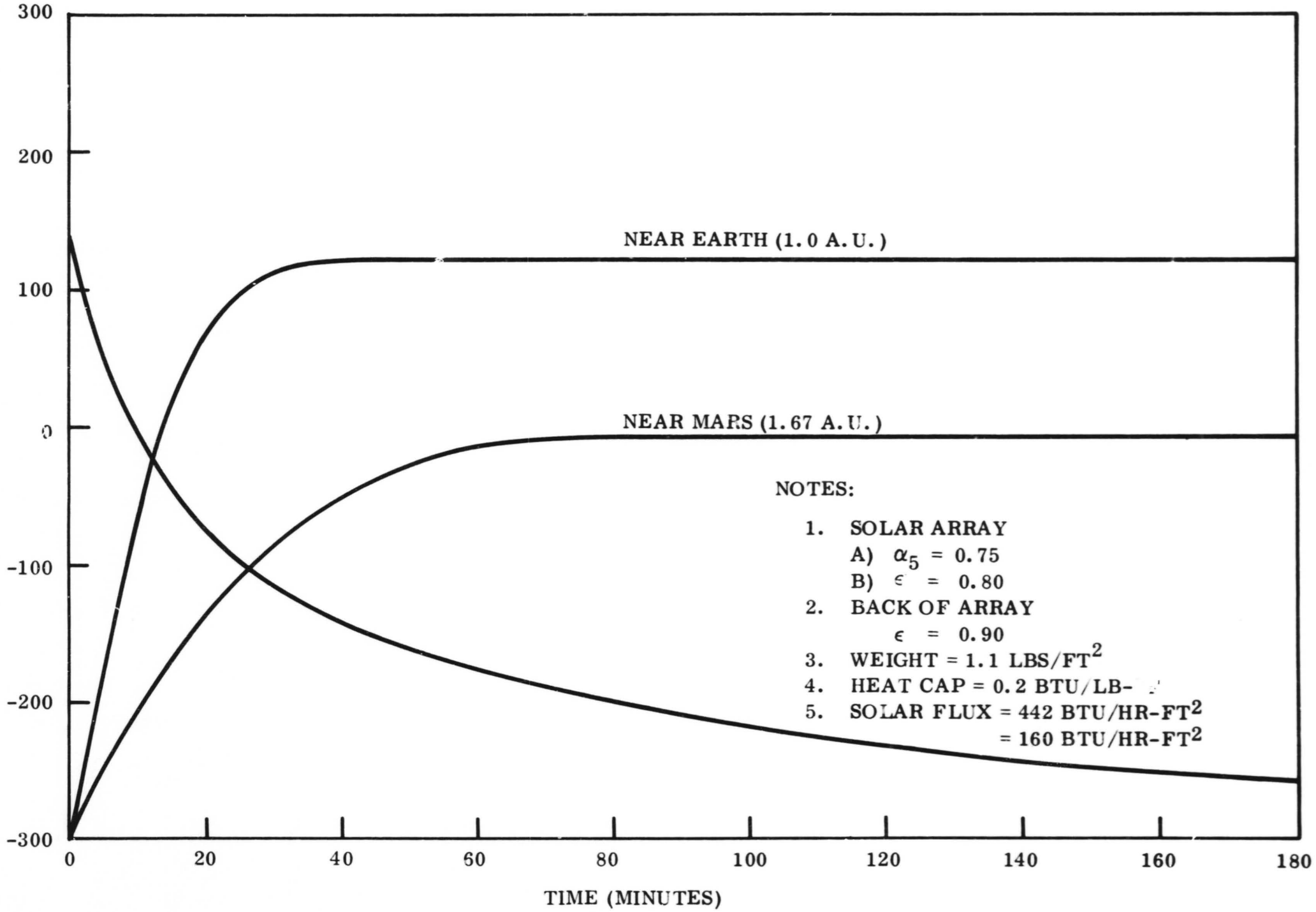


Figure 4.6-12. Solar Array Temperature History During Heatup and Cooldown

- Solar cell arrangement: Number of series cells in upper and lower sections and number of parallel cells.
- Solar cell type
- Solar cell degradation factors
- Solar intensity (AU distance)
- Array temperature
- Array operating voltage
- Minimum load

The outputs are:

- Shunt current
- Shunt voltage
- Shunt thermal dissipation

In effect the program calculates the dissipation shown in Figure 4.6-13.

This calculation was conducted for shunt elements applied to the MM '69 solar panels. The results are shown in Figure 4.6-14 for the conditions specified. The solar cell characteristics used were those described earlier in Section 4.6.3.3 with no allowance for degradation to identify a worst case thermal dissipation. Temperatures were varied over a wide range to simulate possible emergence from a near-Earth solar occultation.

Though one might expect higher dissipation at lower array temperatures when array power is highest, this is not the case as shown on the illustration. A maximum dissipation of 320 watts occurs at about 30^{o}F principally because array currents are higher at higher temperatures.

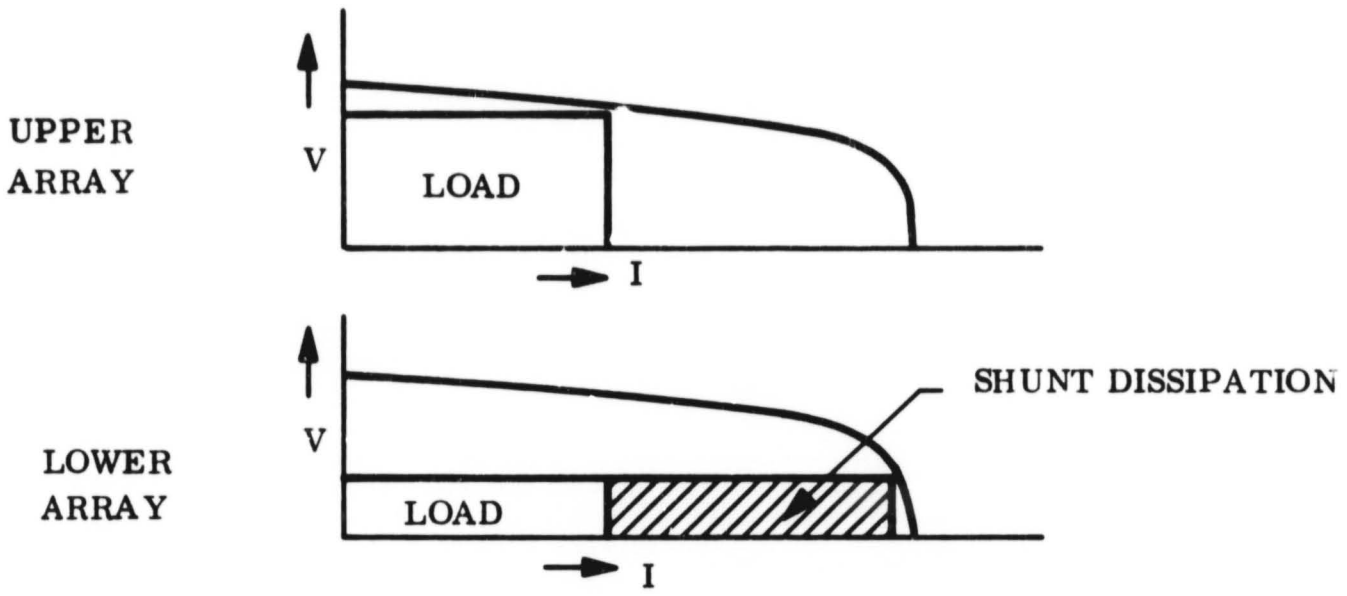


Figure 4.6-13. Partial Shunt Regulator Dissipation

The MM '69 panels use a total of 224, 2 by 2 cm cells. There are 24 strings with 8 strings of 10 paralleled cells and 16 strings of 9 paralleled cells. With a shunt transistor used for each string, the maximum dissipation is associated with a 10-cell string and is:

$$\frac{10}{224} \times 320 = 14.3 \text{ watts}$$

Based on this dissipation, estimates of shunt element temperatures are described below.

4.6.4.3 Shunt Temperature Estimates

As a basis for these estimates, comparisons are first made with the dissipation of the zener diodes used on the MM '69 solar panels. The intent is to examine the ramifications of replacing the six zener diodes used for each string with one shunt transistor at one of the present zener diode locations.

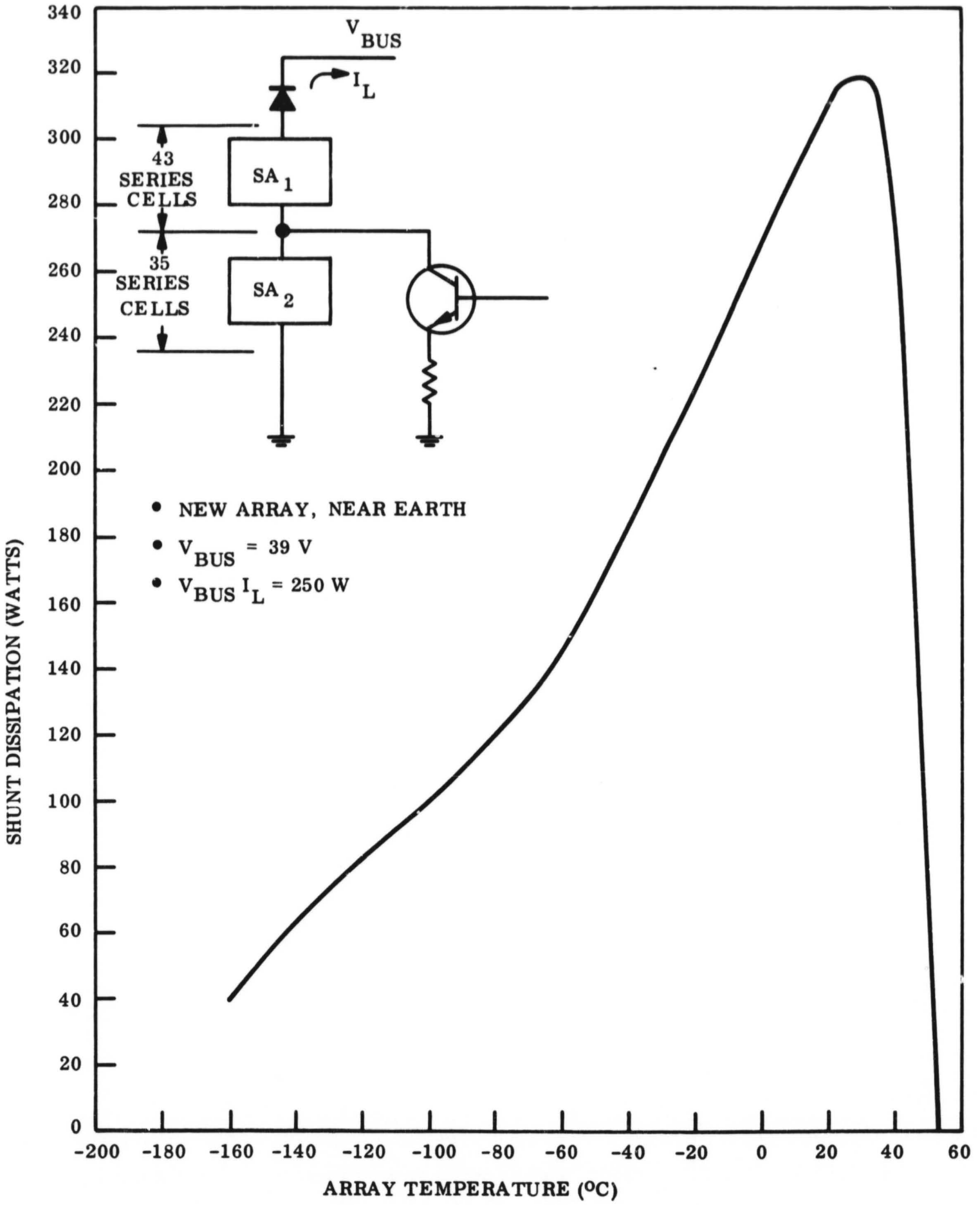


Figure 4.6-14. Shunt Dissipation Versus Array Temperature

The six zener diodes have a cutoff voltage at about 50 volts. In a near-Earth condition with the array very cold after possible emergence from a solar occultation, the array current could be as high as 23 amperes (roughly estimated with the aid of Figure 4.6-9) at 50 volts. With a minimum spacecraft load around 250 watts, this means the zener must dissipate about 900 watts. The zeners for a 10-cell section would then dissipate:

$$\frac{10}{224} \times 900 = 40 \text{ watts}$$

or about 7 watts per zener diode.

The following analysis determines the differences in temperature for the zener diode and shunt transistor dissipations with the objective of determining the need for possible heat sink modification. Emphasis is placed on temperature difference rather than absolute temperature prediction. The latter would have required an extensive evaluation of configuration factor geometry and complex radiation interchange through the many lightening holes in the side members of the MM '69 solar panel box beam spar shown in Figure 4.6-15; these were estimated in the analysis. The temperature distributions given in the following section are considered to be a good indication of the differences in peak shunt temperatures.

Thermal Model

The MM '69 spar box beam configuration with shunt locations is shown in Figure 4.6-15 which is an extract from JPL drawing No. 1000154. The spar is fabricated from 0.020-inch gauge 2024-T4 aluminum alloy with a thermal conductivity of approximately K = 70 Btu/hr-ft-^{o}F. A 31-node thermal model was utilized in the thermal analysis to represent the actual configuration. This is shown in Figure 4.6-16. The lightening holes in the spar were approximated by square holes to simplify the analysis.

An emissivity of 0.9, corresponding to a white or black paint was selected. Both radiation and conductive coupling to the solar array (node 30) at a temperature of 140^{o}F corresponding to a near earth condition, was considered.

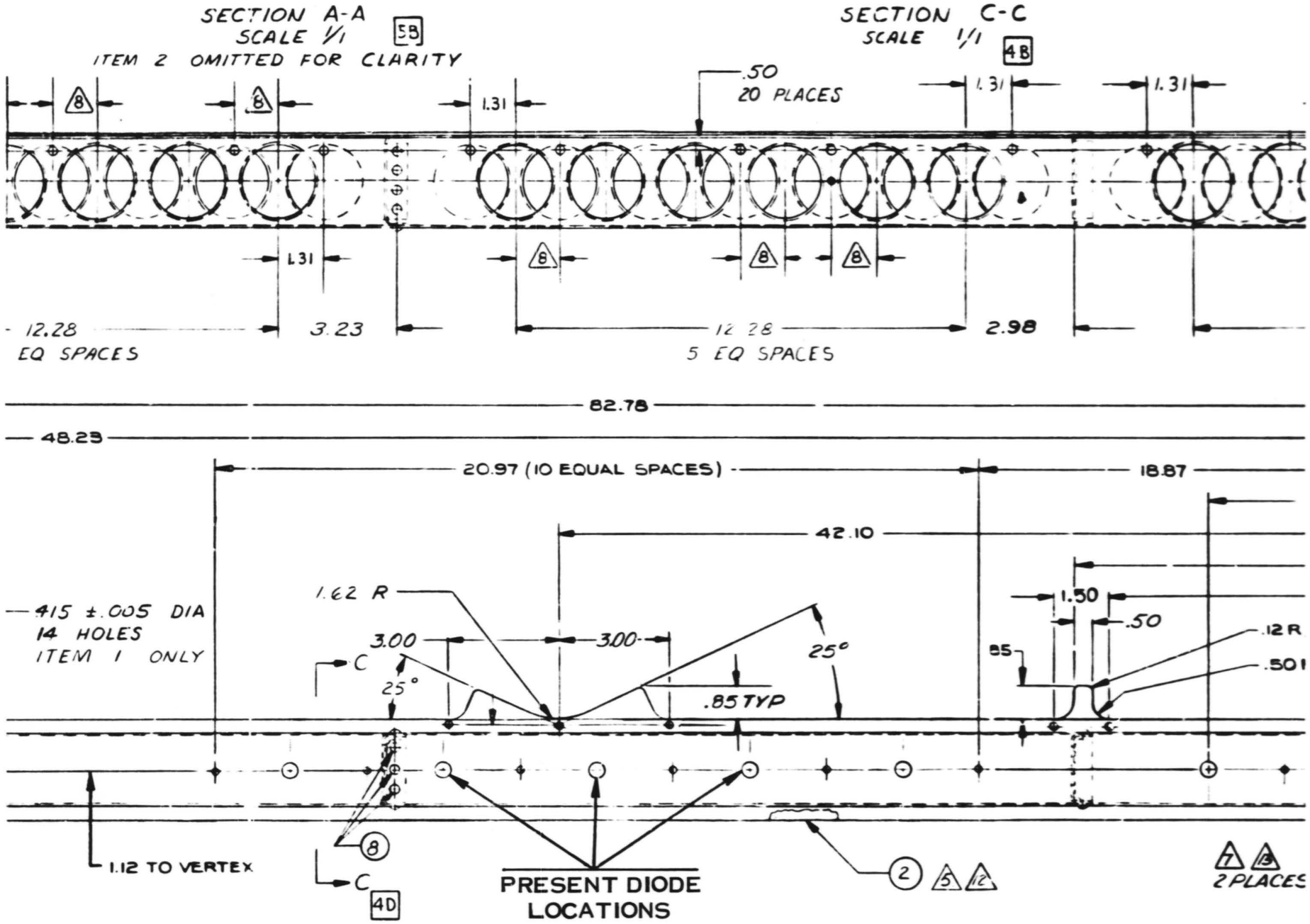
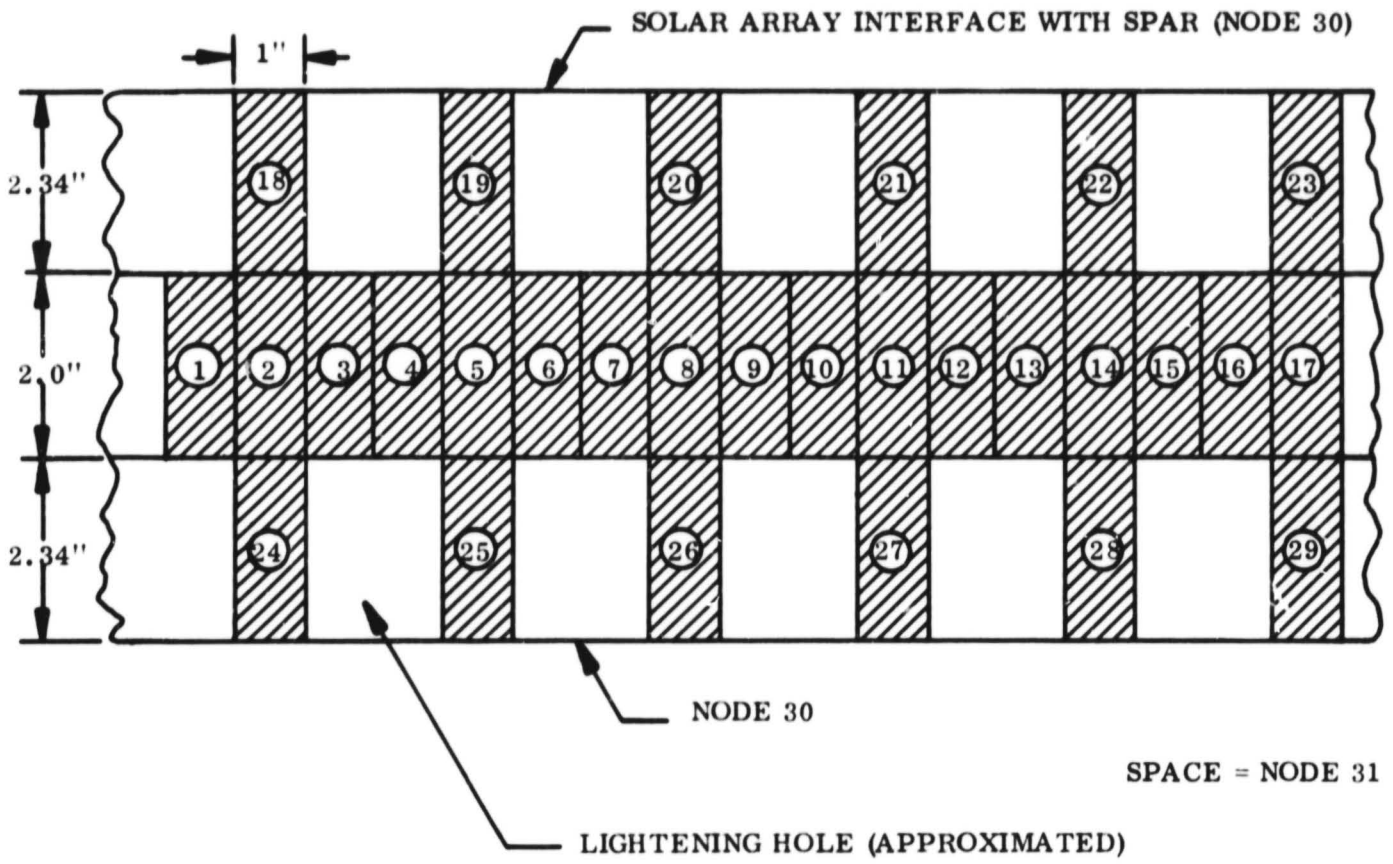


Figure 4.6-15. Dissipation Element Locations



NOTE: SPAR FOLDED OUT ONTO A PLANE

Figure 4.6-16. Thermal Model of Box Beam Spar of Solar Panel

Results

The following four cases were run on the GE 635 digital computer to compare temperature distributions along a section of the spar in the vicinity of the shunt transistors:

a. Three zener diodes located four inches apart and each generating 7 watts -- BASELINE configuration. Three rather than six diodes were considered sufficient to identify local peak temperatures.

b. One shunt transistor at the location of the center zener of case a above which dissipates 14 watts.

c. One, 14-watt transistor (the same as b above) with a 10-inch section (5 inches on either side of the transistor) of the top member of the spar to which the transistor is mounted, increased to 0.04 inch gauge.

d. The same as case c above, except that the 10-inch section was increased to 0.06 inch gauge.

The results are given in Figure 4.6-17 in which steady-state temperatures are given along a section of the spar. The slight asymmetry in the temperature distributions is due to the unsymmetric arrangement of the lightening hole simulation with respect to the shunt transistors. It can be seen that the single 14-watt transistor configuration results in an 80°F increase in peak temperature over the three, 7-watt configuration if the standard 0.02-inch spar gauge is employed. If the gauge is increased to 0.04 inch on 5 inches of either side of the 14-watt shunt transistor, the peak temperature is reduced to the peak level of the three, 7-watt zener diode configuration. By further increasing the thickness to 0.06 inch over the 10-inch spar section, the peak temperature is reduced to a level about 35°F lower than the baseline configuration. In each of the single 14-watt transistor configurations, it is evident that temperatures fall off from the peak more rapidly with distance from the transistor.

Conclusions

It is concluded that one 14-watt shunt transistor configuration can be designed to operate at or below the operating temperature level for the baseline three, 7-watt zener diode configuration by "beefing up" the spar over approximately a 10-inch section surrounding the transistor. The weight penalty associated with an increase from 0.02 to 0.04 inch is 0.04 pounds per spar. The weight penalty incurred by an increase from 0.02 to 0.06 inch 0.08 pound per spar. Some additional weight would have to be added for bonding or brazing the doubler; however, it is considered that in total the weight penalties associated with the thickened sections are almost trivial.

4.6.4.4 Shunt Element Failures

A question of interest in the shunt system is: how many open circuit shunt transistor failures could be tolerated without affecting regulation? The question of short-circuit failures was considered earlier in Section 4.4.4.

To answer the open circuit question, it is necessary to determine the minimum amount of nonshunted solar array that would at some time in the mission just satisfy the minimum possible load. The number of sections associated with this minimum array area are then equivalent to the number of allowable open circuit failures. It is obvious that this occurs at

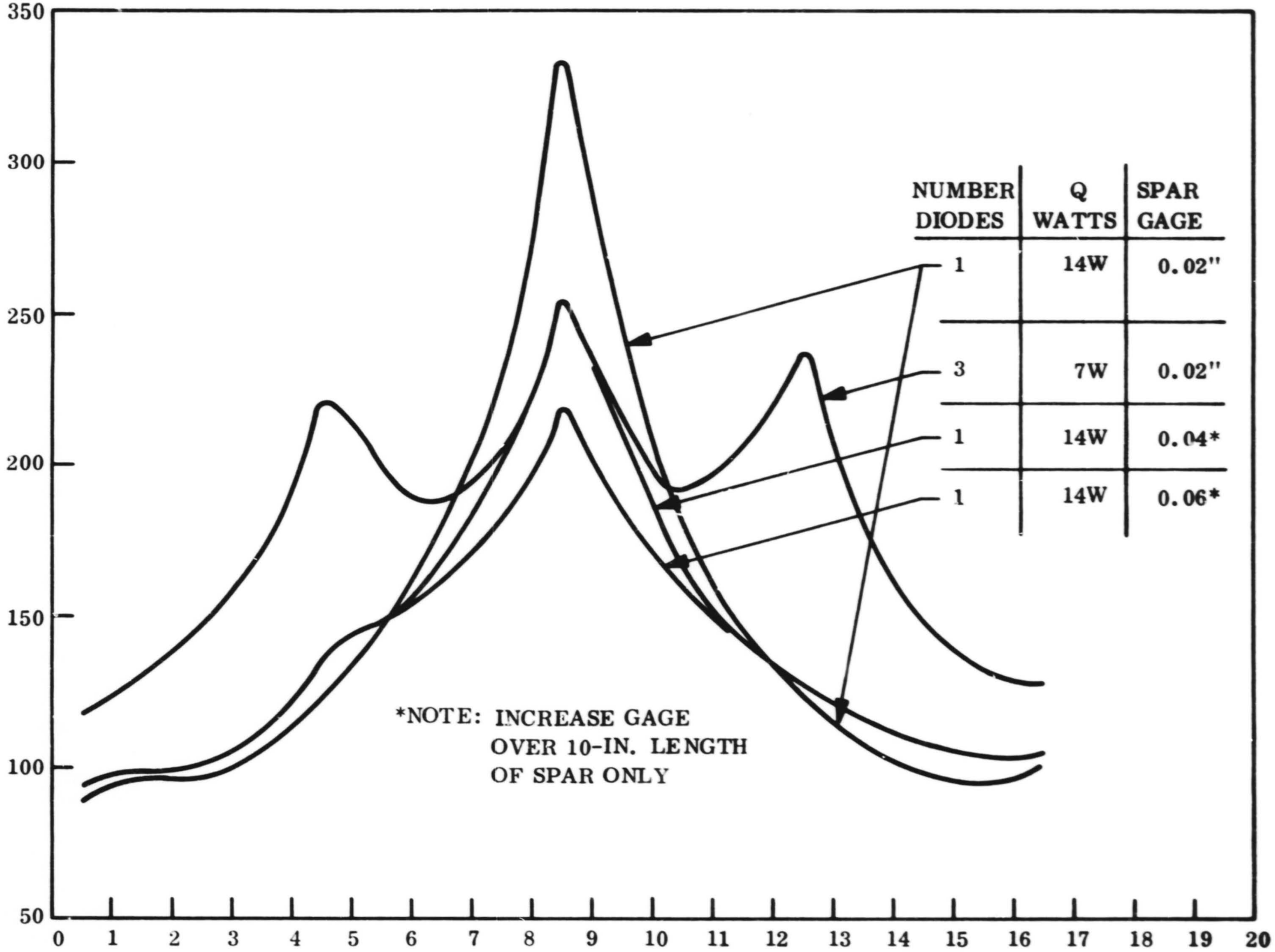
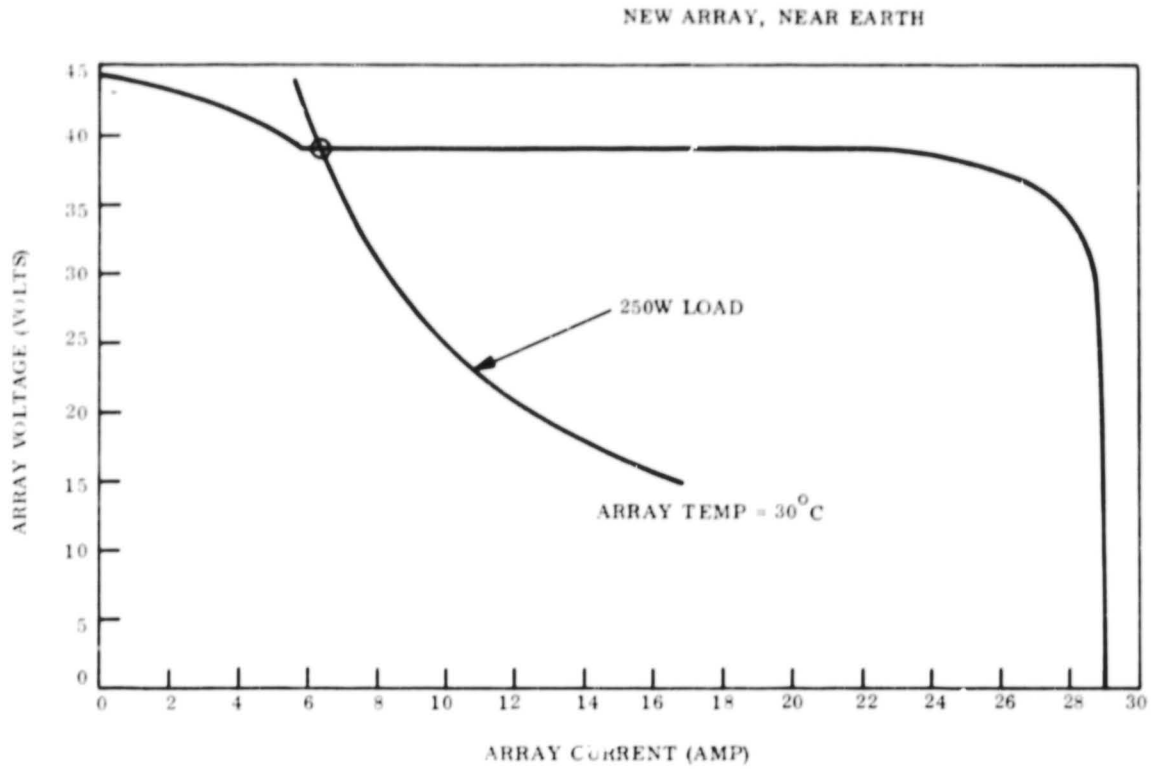


Figure 4.6-17. Spar Temperatures in Proximity of Zener Diodes

near-Earth when power capability is highest. By examining the range of V-I variations with a new nondegraded array, it was found that the equivalent of six sections could provide an assumed minimum load of 250 watts. The maximum capability of these six sections occurs at temperatures of 30°C and -157°C as shown on Figure 4.6-18 which indicates the net V-I characteristic, considering the remaining shunt elements are good.

Thus the shunt system can tolerate about 25 percent open-circuit failures. The overall shunt dissipation decreases proportionately though the dissipation in any single section is unaffected.



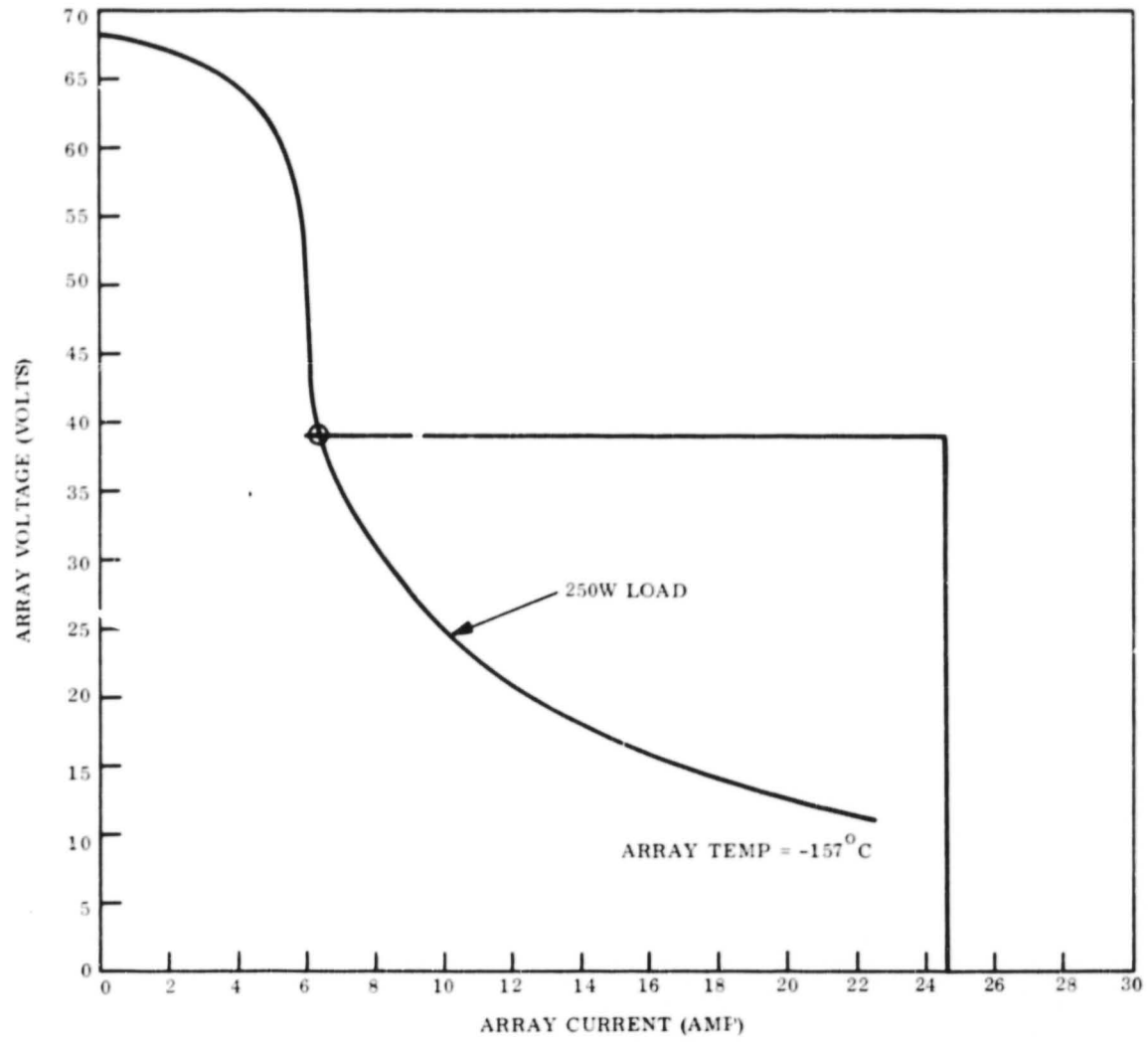


Figure 4.6-18. Array V-I Characteristics with 6 Open Shunt Transistors

4.7 EQUIPMENT DESCRIPTIONS

Equipment characteristics of the shunt regulated system are described in this section. Generally, the equipment can be suitably packaged within the modules defined for the MM '69 system. As a result the equipment is described in terms of changes to the MM '69 equipment modules. As an aid in understanding the extent of necessary module modifications, Figure 4.7-1 shows original equipment allocations for the modules of the MM '69 system, and Figure 4.7-2 shows the identical modules with equipment reallocations for the shunt regulated system.

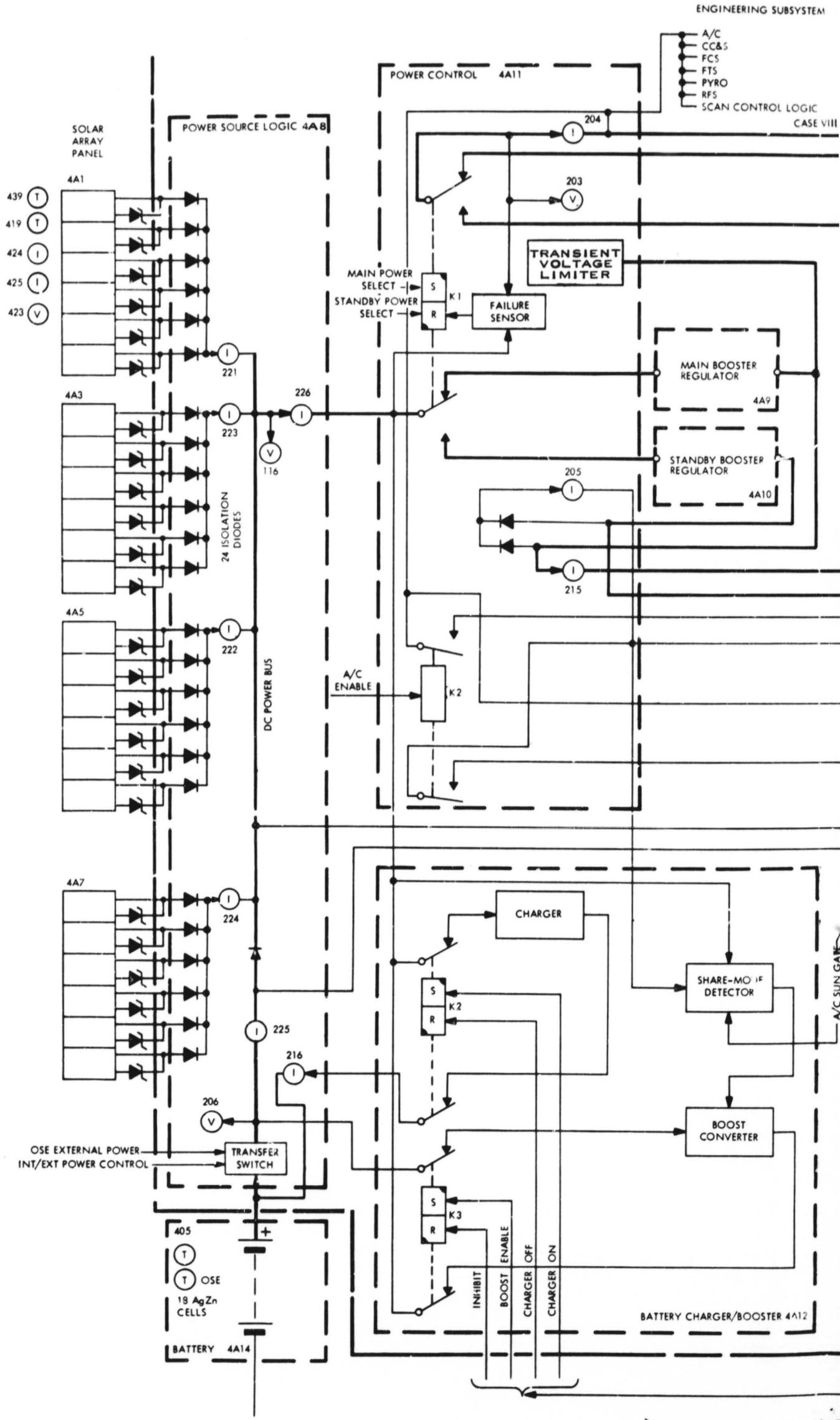
A summary of equipment characteristics is shown on Table 4.7-1 comparing the MM '69 and shunt regulated systems.

Table 4.7-1. Comparison of Equipment Characteristics

Item	MM '69 System	Shunt System
Solar Array		
Gross area	83 ft^2	83 ft^2
No. panels	4	4
No. cells per panel (2 by 2 cm/ N/P 1-2-cm)	4368	4368
No. series cells	78	78
No. parallel cells per panel	56	56
Voltage limit	53 volts max (zener diodes)	39 volts max (Active shunt)
Battery		
Cell type	Ag - Zn	Ag - Zn
No. series cells	18	18
Nominal ampere-hour capacity	50	50
Boost Regulator		
Output power rating	250 watts	260 watts
Input voltage	25 - 50 volts	25 to 38.2 volts
Output voltage	56 $\pm$ 1% volts	37.5 $\pm$ 1% volts
Nominal efficiency at rated power	84 to 89%	84 to 89%
Overload rating	376 watts - 1 msec	390 watts - 0.1 sec

Page intentionally left blank

FOLDOUT FRAME 1



FOLDOUT FRAME

FOLDOUT FRAME 2

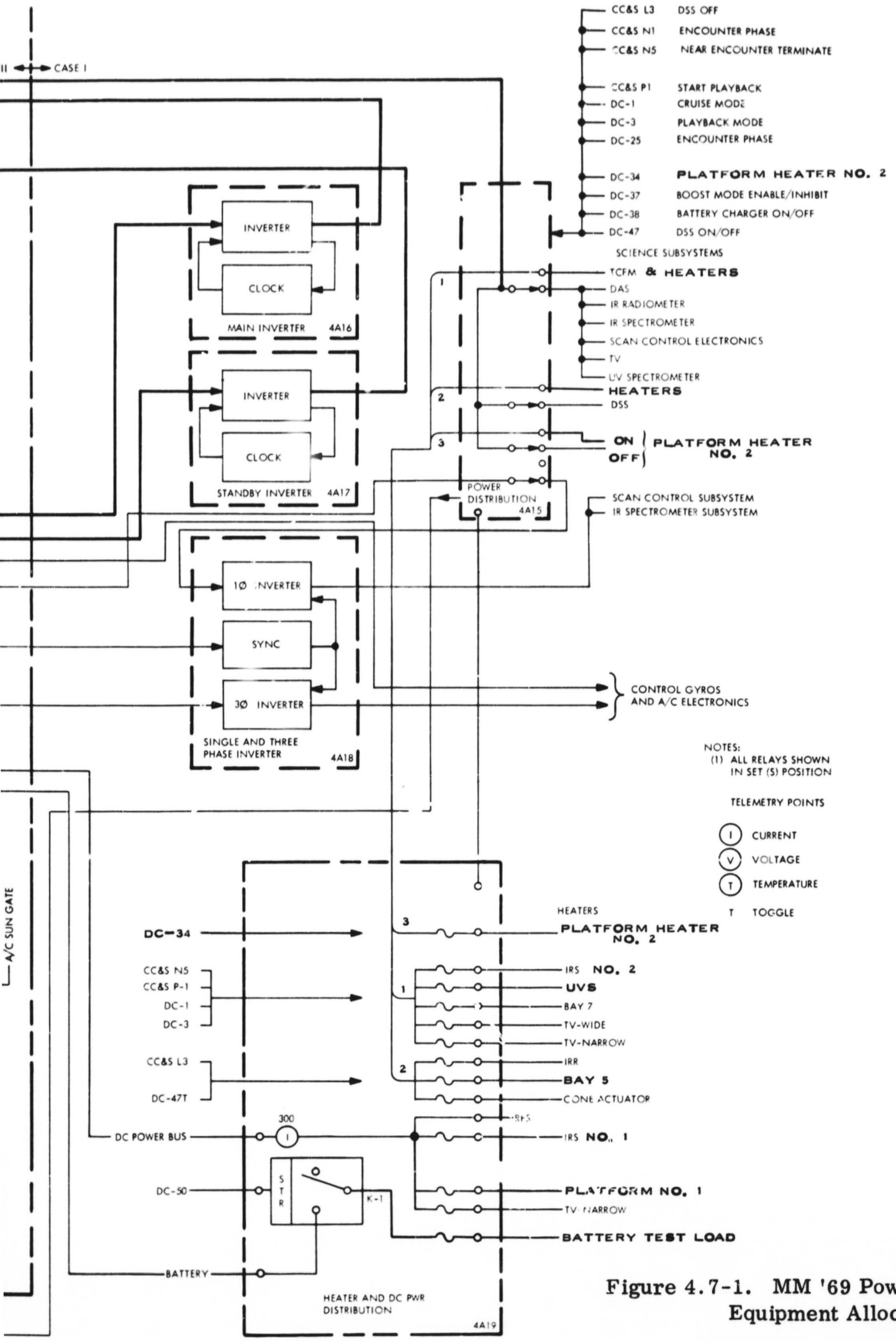
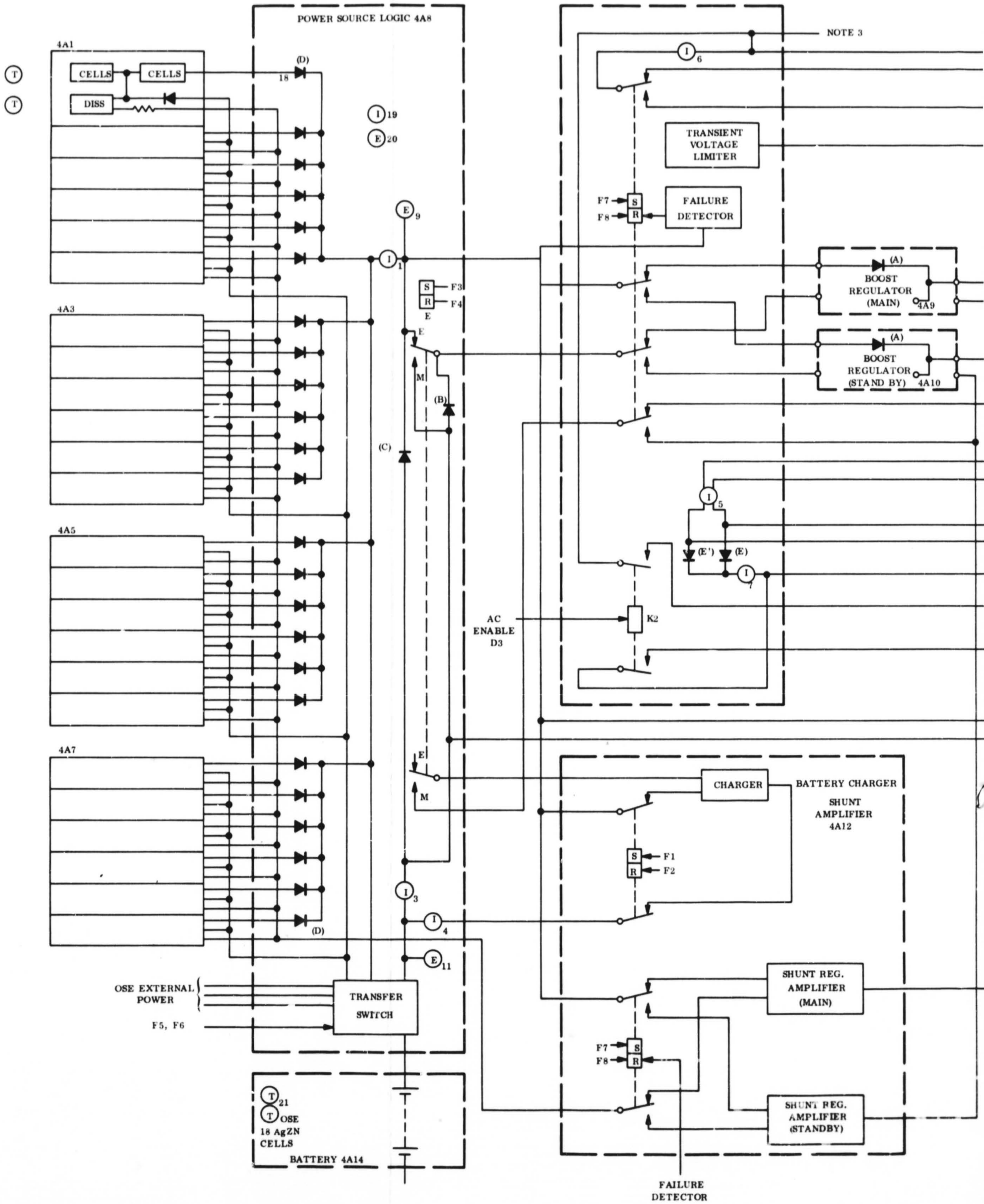


Figure 4.7-1. MM '69 Power System Module Equipment Allocation

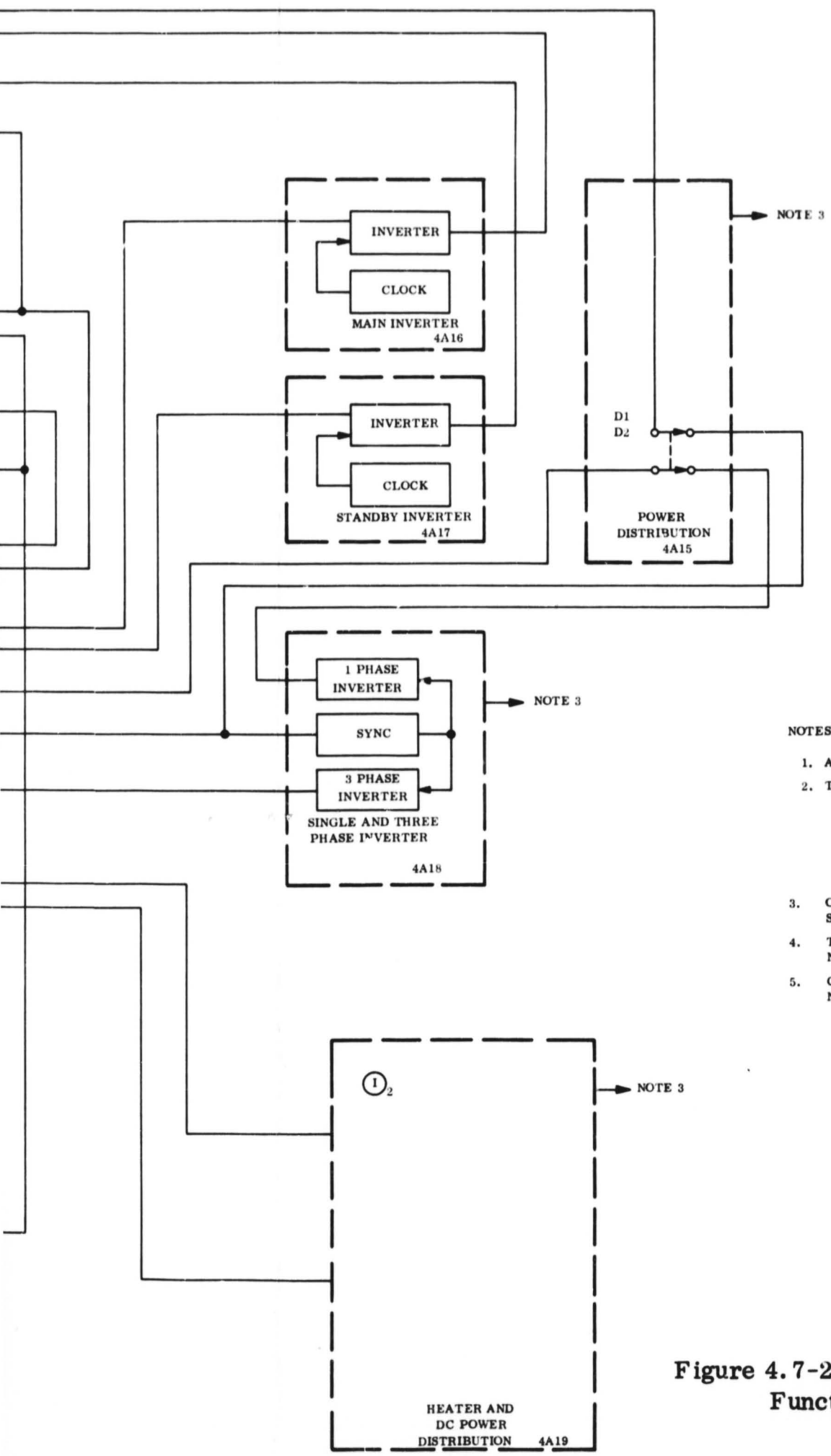
FOLDOUT FRAME

FOLDOUT FRAME 3



FOLDOUT FRAME

FOLDOUT FRAME 4



NOTES:

1. ALL RELAYS SHOWN IN SET POSITION
2. TELEMETRY POINTS
   - I CURRENT
   - E VOLTAGE
   - S DIGITAL
   - T TEMPERATURE
3. OTHER INPUTS AND OUTPUTS ARE AS SHOWN ON FIGURE 4.4-1.
4. TELEMETRY SUBSCRIPTS REFER TO ITEM NO. IN TABLE 4.9-1.
5. COMMAND SUBSCRIPTS REFER TO ITEM NO. IN TABLE 4.9-2.

Figure 4.7-2. Shunt Power Subsystem - Functional Block Diagram

FOLDOUT FRAME

containing 78 solar cells in series. Four sections contain nine paralleled solar cells, and two sections contain ten paralleled solar cells. Twenty-mil fused silica cover slips are bonded to each solar cell. Each section is voltage limited by a series string of six zener diodes wired across the negative and positive output terminals. The zener diodes are heat sink mounted on longitudinal box beams forming part of the structural substrate of the panels. A solar cell experiment module consisting of several individual cells and associated telemetry transducers is also mounted on each panel.

Changes in the solar array for use in the shunt regulated system are noted below:

- The six zener diodes wired in series for each array section are removed and replaced with a single shunt transistor. Each transistor is wired from the negative terminal of the section to the positive terminal of the 35th series element as shown on the schematic of Figure 4.7-3, 4.7-4, and 4.7-5. The solar cell layout shown is identical in every respect to the MM '69 layout, including the terminal breaks shown along the various rows. By examination, it may be seen that the transistors are tapped at available string terminations, and therefore no layout modifications are necessary.

- The shunt transistors selected for the application are type MHT 8070 manufactured by Solitron Devices, Incorporated. They were selected on the basis of gain, temperature, and radiation resistance characteristics (see Section 5.3.1). The transistors are stud-mounted devices and mounted on the panel spars, as were the zener diodes. It may be necessary to locally increase the span thickness for heat sink purposes (see Section 4.6 .4).

- Base drive isolation resistors are required for each shunt transistor. Five-watt chassis mounted resistors are appropriate for this purpose.

- Test diodes are required in the circuit configuration shown. Unitrode 2-ampere diodes are selected for this purpose. The test procedure is described in Section 4.10.

- Harness and connector changes will be required to accommodate the above modifications.

4.7.2 POWER SOURCE LOGIC (PSL) - MODULE 4A8

As shown on Figure 4.7-1 the MM '69 PSL module serves to transfer power from the solar array, battery, and OSE supplies. It contains the solar array isolation diodes, certain power subsystem telemetry sensors, and the internal/external power switch.

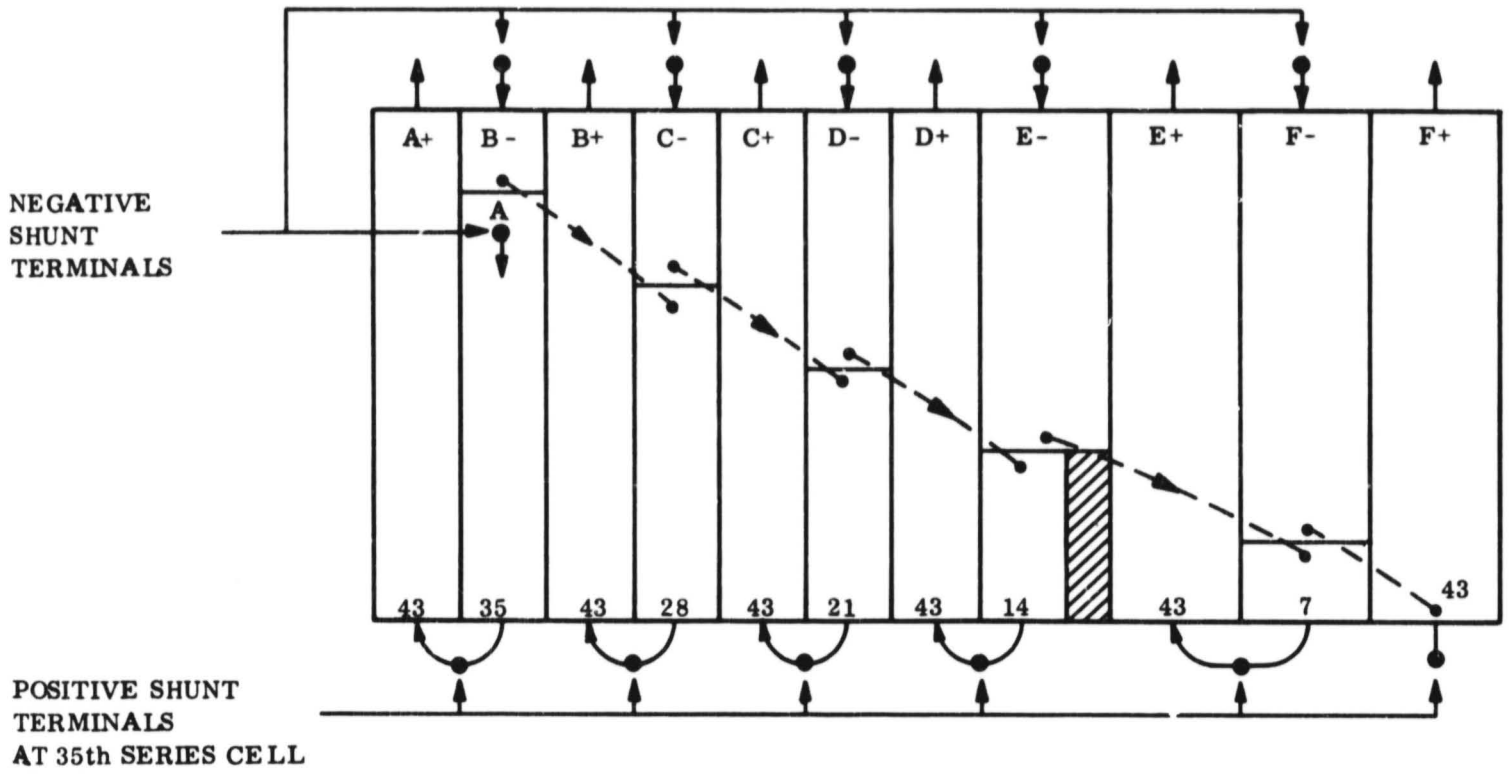


Figure 4.7-3. Panel Harness Rearrangement to Accommodate Shunt Transistors at 35th Series Cell - MM '69 Panel

Changes in the PSL module required for the shunt regulated system are summarized below:

- Add the Earth/Mars mode relay
- Revise telemetry measurements as shown on Figure 4.7-2 and as described in Section 4.9
- Add battery discharge diode (B)

The major change from the MM '69 PSL is the addition of the Earth/Mars mode relay. This relay is physically added to this module because the relay contacts connect directly to power distribution diodes already located in this module. Some repackaging design will be required. Use of piece part redundancy for this switch should be considered in Phase II (see Section 5.2.7 and 5.2.9.2). A weight increase of 0.12 pounds is estimated for the PSL module.

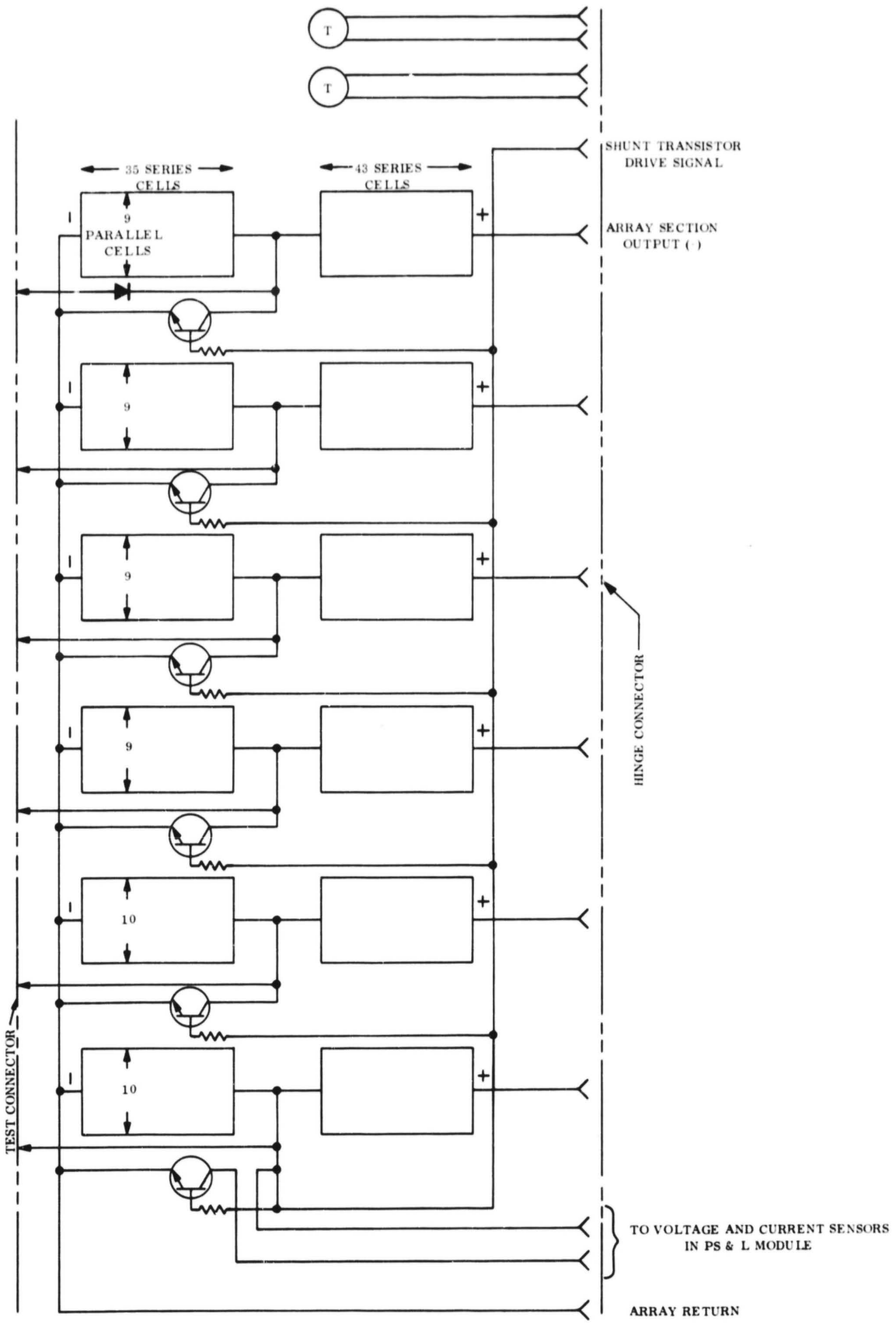


Figure 4.7-4. Single Mariner Panel Schematic, Shunt Regulator System

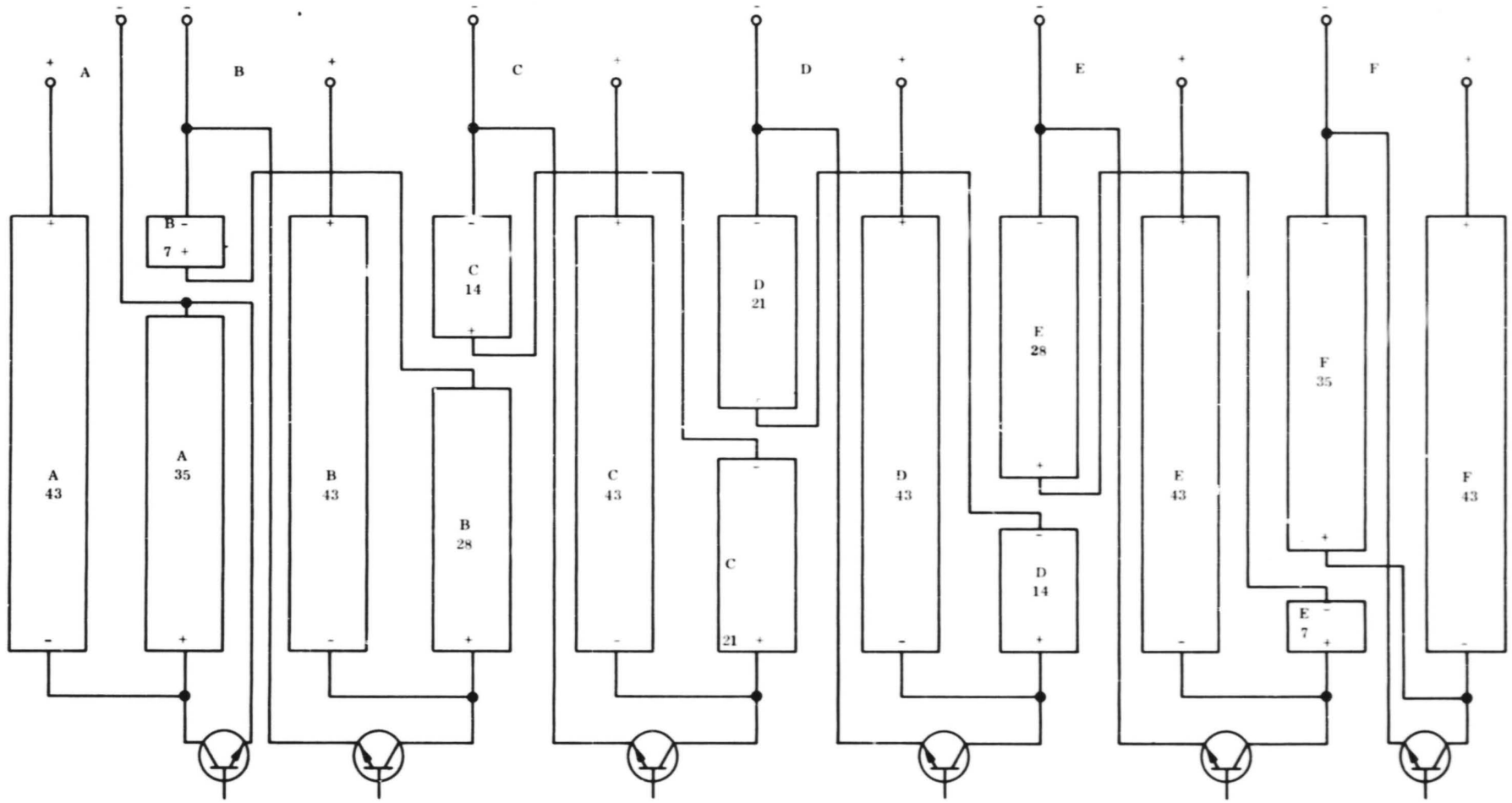


Figure 4.7-5. Single Mariner Panel Schematic, Shunt Regulator System

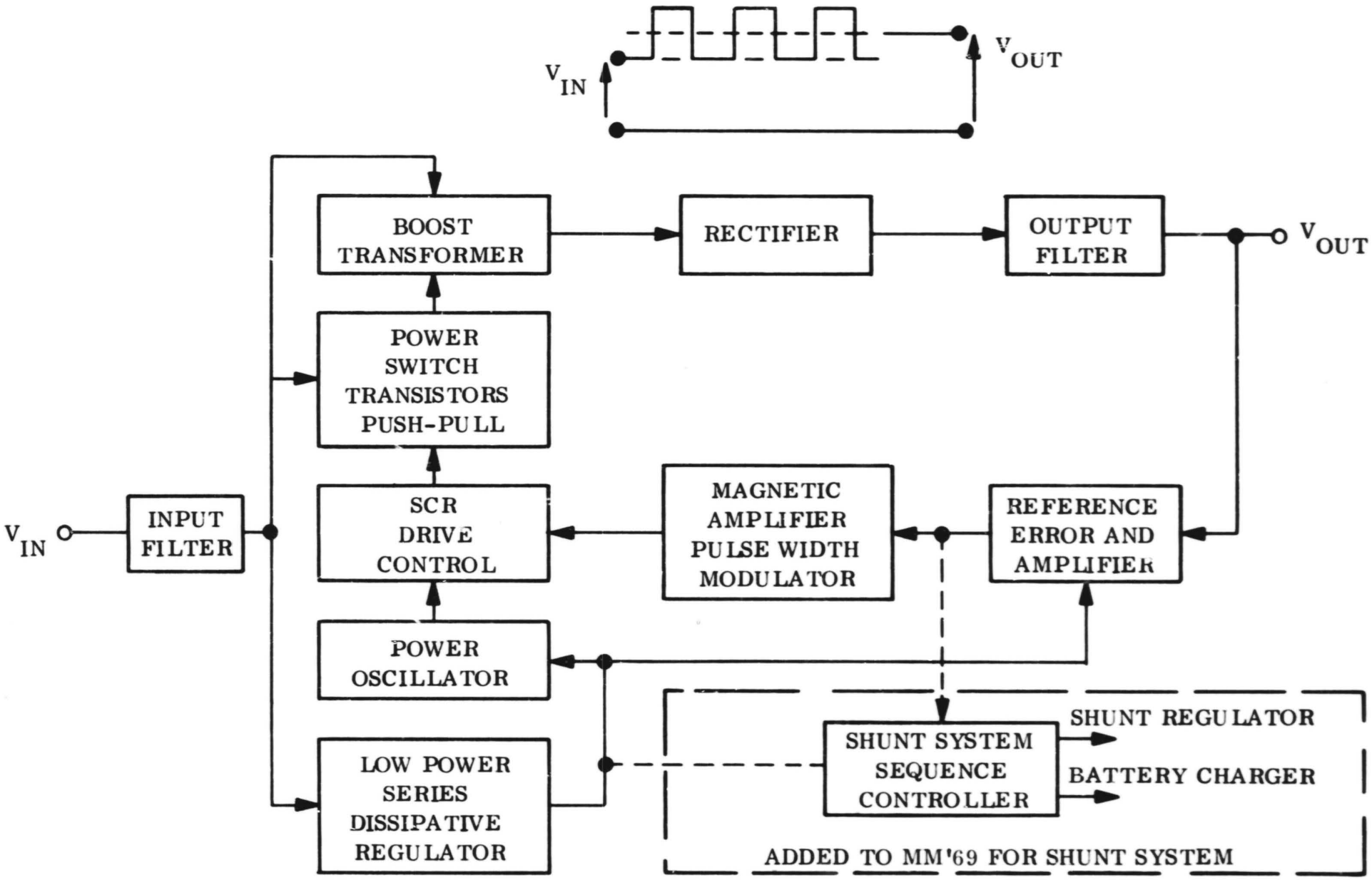


Figure 4.7-6. MM '69 Boost Regulator Block Diagram

4.7.3 BOOST REGULATOR, MAIN AND STANDBY - MODULES 4A9 AND 4A10

The MM '69 boost regulator has an output rating of 250 watts and conditions the unregulated power from the solar array and battery (25 to 50 vdc) to a regulated output at 56 vdc ±1 percent. The regulator is pulse width modulated as shown in the block diagram of Figure 4.7-6. The indicated changes required for the shunt regulated system are described later. The power switch transistors operate at a constant frequency with a variable duty cycle determined by the output voltage. At low output voltages, the duty cycle (or pulse width) is increased; at high output voltages, the reverse occurs with a reduced duty cycle. The input voltage is boosted by the switch action of the transistor and boost transformer. The boosted voltage adds to the input voltage and is then rectified. The rectified voltage wave shape feeding the output filter is also shown. The output filter averages the pulsed voltage wave shape to provide a dc output voltage having a low ripple. The low power dissipative regulator is provided for constant drive current to the power transistors and to assure constant frequency operation.

The necessary changes to the boost regulator for use in the shunt regulated system are summarized below:

- Increase output power from 250 to 260 watts --based on load profile
- Decrease output voltage from 56 volts to 37.5 volts -- based on array power at Mars
- Increase transient overload capability from 0.0001 to 0.1 seconds -- based on load fault/fuse size requirements
- Isolate low power circuits from battery when in Mars Mode operation -- prevents battery from discharging due to standby power required by boost regulator
- Add isolation diode -- required as part of shunt system implementation
- Add sequence controller -- circuit duplication is avoided since present regulator has similar functions

The small output power increase has little effect on boost regulator size or performance. However, the lower output voltage requires a higher output current with possible changes to the output filter to maintain efficiency and size. It is possible to maintain both size and efficiency with an increase in oscillator frequency by a factor of four*. The lower output voltage permits a smaller boost transformer because the percent of total power transfer by the boost transistors is reduced. This lower power also results in the desired increased transient overload capability. Low power circuits are isolated from the battery through diode isolation as shown in Figure 4.7-7. The only power required from the battery is power transistor leakage.

The addition of the isolation diode requires repackaging; thermally, its location may be on the same heat sink as the boost power transistors because the diode and power transistor operations tend to alternately dissipate power. The addition of the sequence controller also requires repackaging; however, little volume is required since the circuits are low power signal type circuits. Figure 4.7-8 is a schematic diagram of the sequencer.

The total effect of these changes on size and weight is an increase in weight (0.066 lb) due to the isolation diode and a decrease in weight (0.062 lb) due to the power transformer change for lower output voltage.

Depending on how redundancy for the 400 Hz inverter is applied (see Section 4.4.2) and possibly for test reasons, overload protection for the boost regulator may be desirable. Figure 4.7-7 shows the additional parts required to incorporate such protection. With excessive load, the transistor duty cycle would be controlled to limit output current. When the

---

*This factor is based on the need to reduce choke resistance which implies either larger wire and core or fewer turns on the same core. The choke current is 1.5 times the original level. The new power loss is $(1.5)^2 R_O = P = 2.25 R_O$. To keep the copper loss constant, the resistance must decrease by 1/2.25. Using the same core the copper area remains constant requiring that the turns must decrease by at least two. The corresponding inductance will decrease by a maximum of 4. Therefore, for the lower inductance to be sufficient, the oscillator frequency may have to increase by the square of the change in turns ratio (4 maximum).

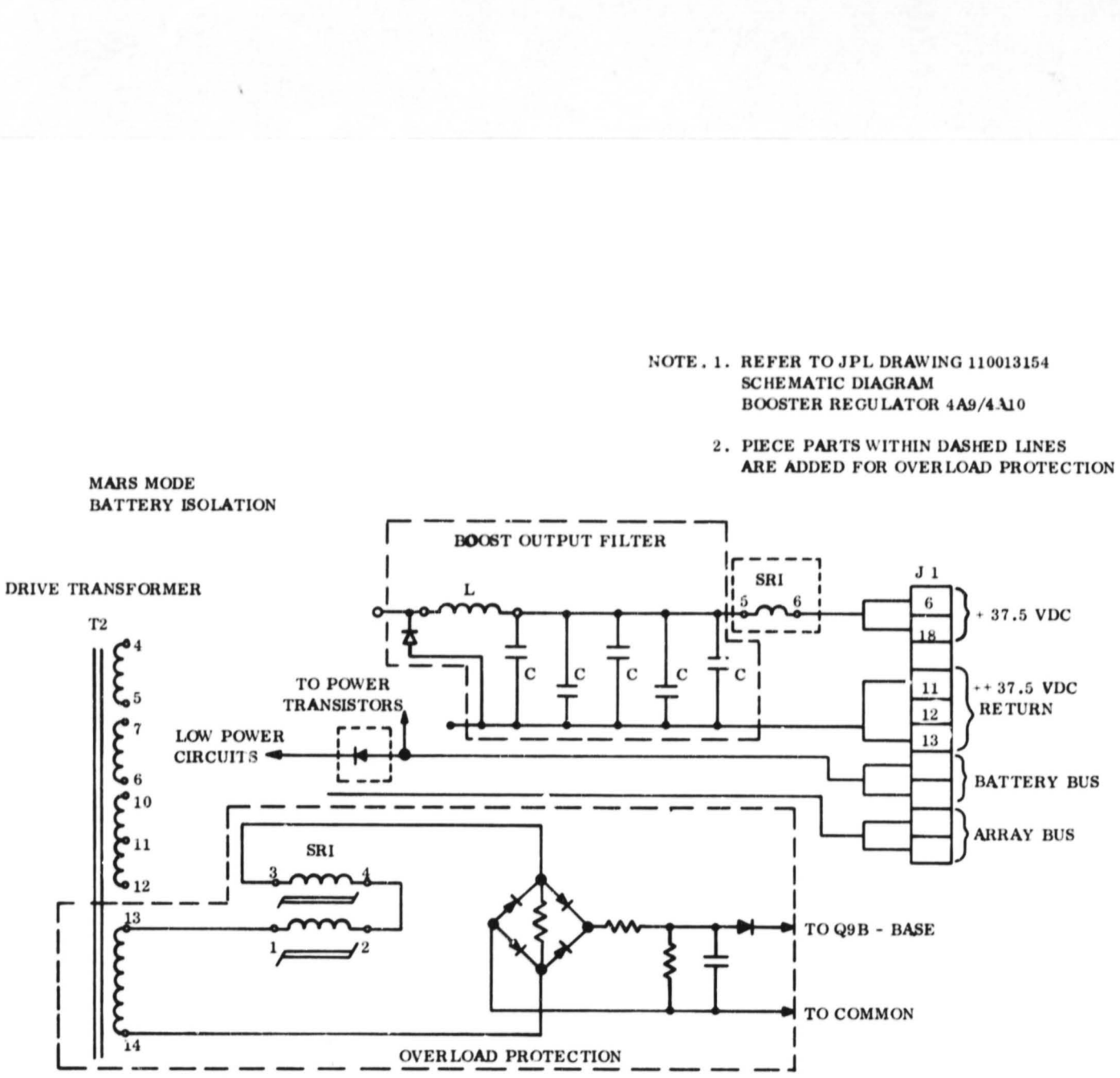


Figure 4.7-7. Boost Regulator Overload Protection Circuit Diagram

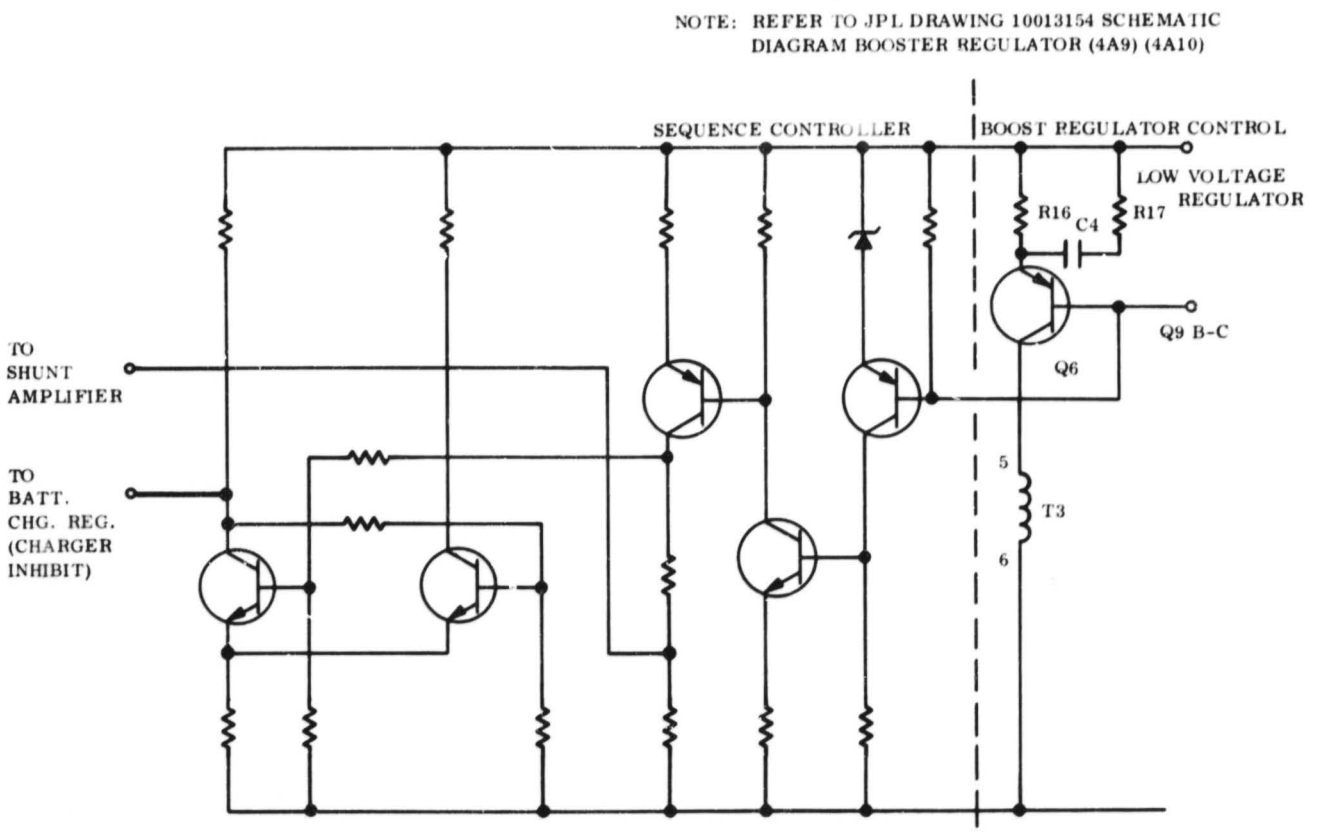


Figure 4.7-8. Sequence Controller Schematic Diagram

transistors are fully off, the output voltage would be depressed to the battery discharge level with the resulting possibility of fault sensor transfer. All of the load fault/fuse size criteria established in Section 5.1.5 are pretinent in avoiding this possibility.

To maintain size and efficiency, the series inductance was reduced with a corresponding increase in operating frequency. Reduction of the equivalent series inductance along with modification of the control circuits (as discussed in Section 5.1.5.1) should improve the transient response of the boost regulator.

4.7.4 POWER CONTROL --- MODULE 4A11

The MM '69 power control module contains the failure sensor for the main power chain, the power transfer relay for the main power chain (boost regulator and 2.4 kHz inverter), the A/C enable relay supplying power to the ACS, power logic diodes supplying power to the ACS, power logic diodes supplying power to the single and three phase 400 Hz inverters, certain power subsystem telemetry sensors, and a transient voltage limiter circuit. Figure 4.7-9 shows the functional circuit block diagram of the MM '69 failure detector which monitors output voltage deviations of the main power chain. Power for the failure detector is supplied from the unregulated bus and is regulated for the over and undervoltage detectors, time delay, and relay drive circuits. The regulated dc voltage is monitored for boost regulator output out-of-tolerance voltages. The 2.4 kHz inverter output is monitored through a tuned filter for out-of-tolerance frequency. The over and undervoltage detectors compare these signals with a reference voltage and operate in conjunction with a Schmitt trigger circuit having appropriate hysteresis so that the time delay actuates the relay driver causing a transfer to the standby chain.

The necessary changes to the power control module for use in the shunt regulated system are summarized below:

- Modify failure detector--based on shunt power system failure criteria--Section 5.1.4 and 5.2.6, Case I

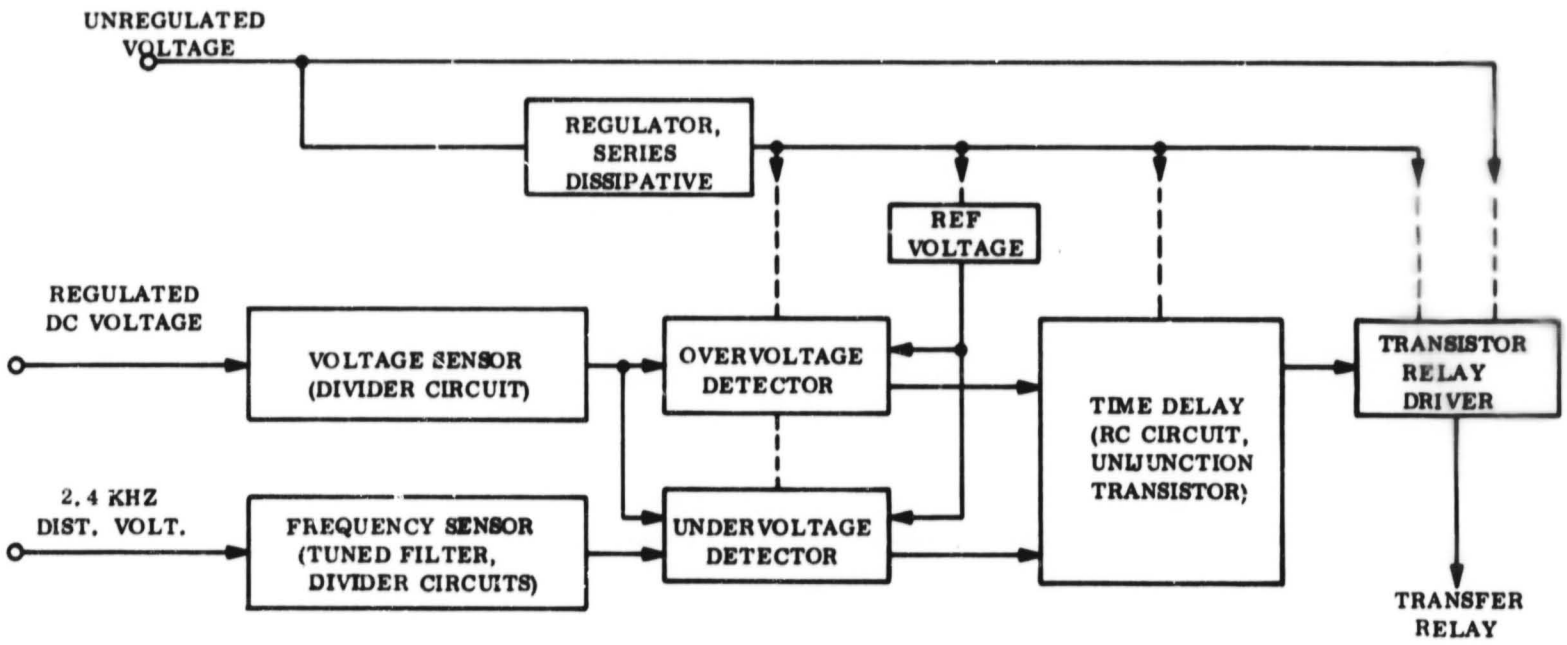


Figure 4.7-9. MM '69 Failure Detector Block Diagram

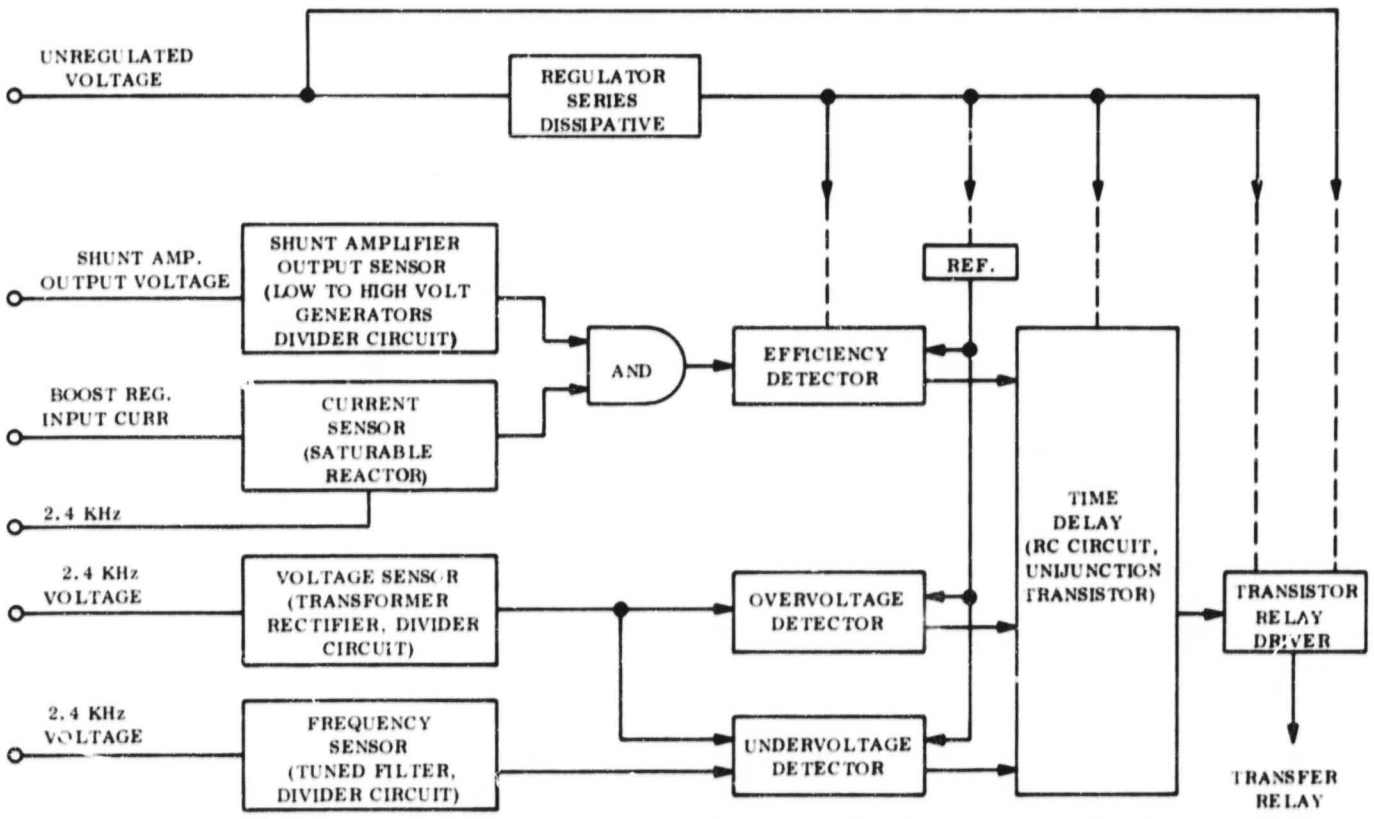


Figure 4.7-10. Failure Detector Block Diagram

- Increase the number of contacts for the fault transfer power relay
- Reduce the voltage limit of the transient voltage limiter because of a reduction in regulated voltage from 56 to 37.5 volts
- Modify the range of telemetry sensors as described in Section 4.9

The major change is the tentative addition of the system efficiency sensor as shown in Figure 4.7-10. The current sensor is shown in this module for purposes of defining the failure detector through it may be better to locate the current sensor with the boost regulator. The excitation for this sensor is taken directly from the 2.4 kHz distributed voltage.

The output voltage from the shunt amplifier is normally very low when the shunt regulator is off. Further, the output voltage does not have to rise very much ($\approx$ 1.5 volts) to cause the shunt regulator to dissipate power. Low voltage detector circuits are difficult to devise. Investigation will be required to establish suitable circuits. One approach would be an amplifier with a constant gain. The actual circuit selection is deferred until Phase II. It is also possible that the efficiency detector requirement may be eliminated if a low efficiency condition without voltage deviation cannot be demonstrated by test.

The output voltage sensors are removed from the regulated dc voltage (inverter input) and relocated at the inverter output voltage to detect possible failures within the inverter.

The frequency detector is located at the inverter output in a similar fashion to that used in the MM '69 approach.

These changes result in a weight increase of 0.16 pounds.

4.7.5 BATTERY CHARGER/BOOSTER -- MODULE 4A12

The MM '69 battery charger/booster module contains the battery charger, boost [illegible]verter, share mode detector, and power transfer relays. The charge regulator limits charge current to the battery to 1.0 ampere maximum and limits the battery terminal voltage to 34.6

(±.2) volts. Charge is terminated by command through the charger power transfer relay. The boost converter, when enabled by the share mode detector, raises the unregulated solar array/battery bus to approximately 50 volts. This occurs when the unregulated bus is between 30 and 33 volts and when the solar array is sun oriented. The power pulses applied to the unregulated bus force the array operating point out of a share mode with the battery. Figure 4.7-11 shows the MM '69 charger functional block diagram. Block diagrams and further disscussion of the boost converter and share mode detector are not provided since these functions are eliminated in the shunt power system.

The necessary changes to the 4A12 module for use in the shunt regulated system are summarized below:

- Remove boost converter and share mode detector--not required in the shunt regulated system
- Modify charge regulator
    a. Increase current limit to 2.0 amperes
    b. Provide two-step voltage limit control at 35 and 33.6 volts
    c. Provide means for charge inhibit signal from sequence controller
- Add main and standby shunt regulator preamplifiers

A block diagram of the charge regulator is shown in Figure 4.7-12. Except for the two-step voltage limit control, it is similar to the MM '69 charge regulator. During charge the current is limited to 2.0 amperes. When the 35-volt limit is reached, the current reduces as determined by the battery impedance characteristics. When it is reduced to 50 milliamperes (at 35 volts), the charger automatically reduces the voltage limit to 33.6 volts causing a further reduction in current whose level is again determined by the particular battery impedance characteristics. This is done to reduce electrochemical stress on the battery after it is fully charged. The reduced battery voltage of subsequent battery demands automatically resets the voltage limit to the higher value permitting normal recharge after the battery demand period is terminated. The two-step approach serves as a backup to normal command turn-off of the charger.

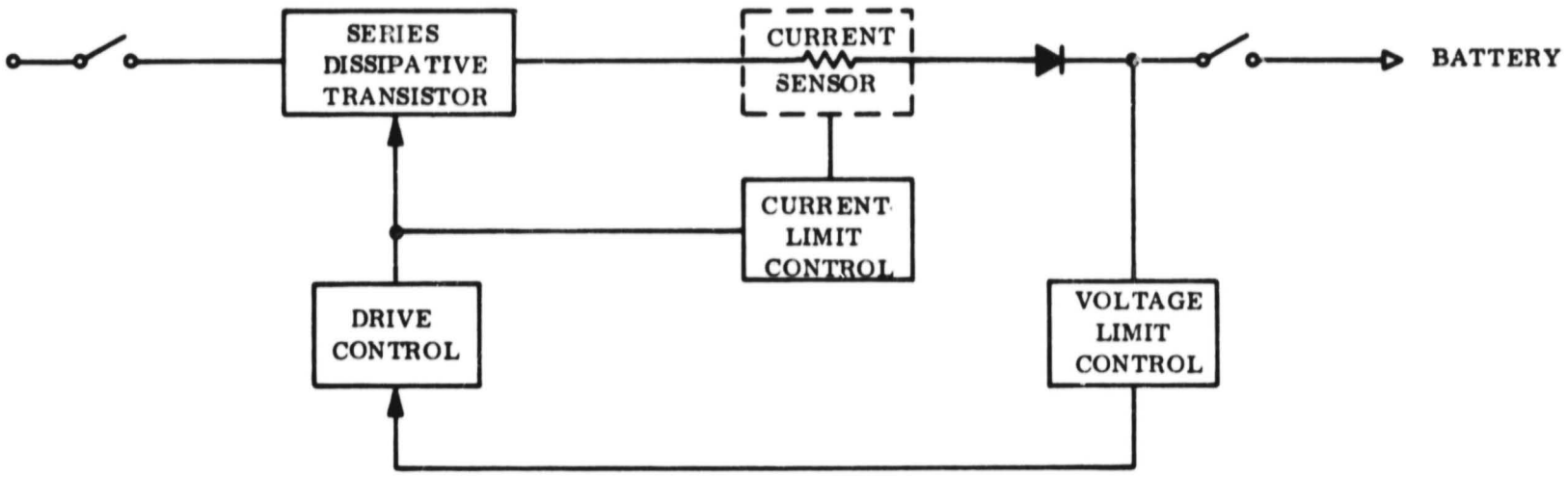


Figure 4.7-11. MM '69 Battery Charge Regulator Block Diagram

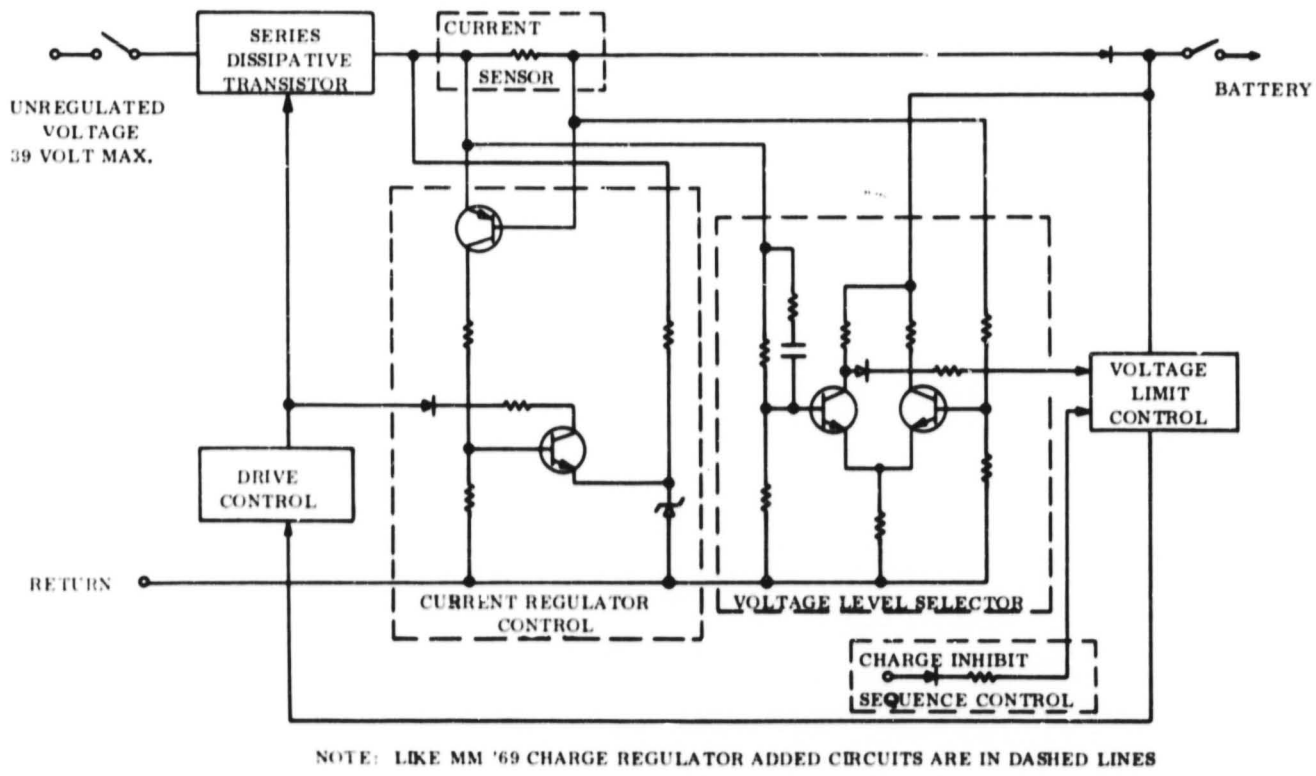


Figure 4.7-12. Battery Charge Regulator Diagram

The battery charge inhibit signal pertains to the signal provided by the sequence controller during array power limited situations with the system in the Mars mode of operation.

The main and standby shunt regulator preamplifiers are identical. One operates with the main power chain and the other with the standby power chain. The shunt amplifier receives its input signal from the boost regulator sequence control. Figure 4.7-13 shows a schematic diagram of these shunt amplifiers. The power dissipation of the shunt amplifier output transistor may be as high as 10 watts. With a maximum input of 38.5 volts and a current limit of 2 amperes, the charge regulator dissipation is about 7 watts for a 35-volt charging level. Thus, the module thermal dissipation will be about 17 watts. The MM '69 charge regulator has a 1-ampere current limit but may receive an input as high as 50 volts with a resulting thermal dissipation of 15 watts, again using a 35-volt charging level. Thus, the difference in thermal dissipation for the two cases does not appear large although this should be further examined during a Phase II effort.

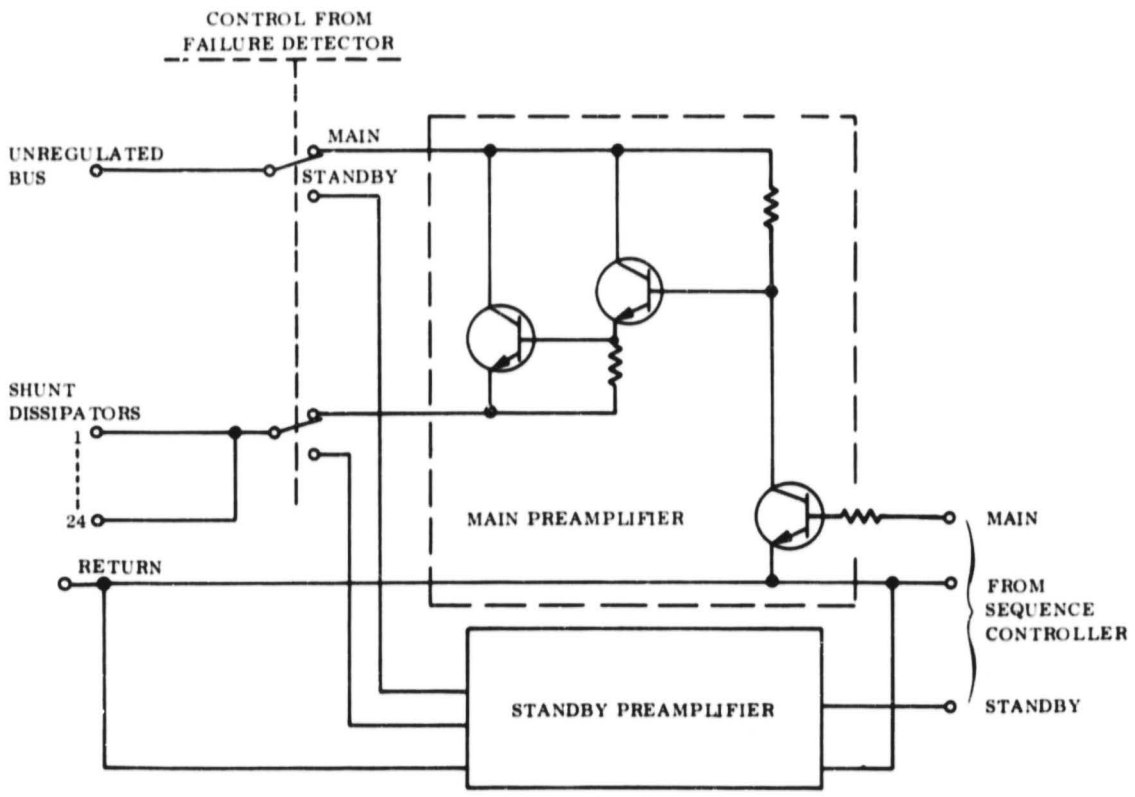


Figure 4.7-13. Shunt Regulator-Shunt Amplifier Schematic

4.7.6 BATTERY - MODULE 4A14

The MM '69 battery consists of 18 silver-zinc cells in series with a nominal capacity rating of 50 ampere-hours.

As indicated in earlier discussions, the MM '69 battery appears adequate for the shunt regulated system considered in this study.

Battery life requirements are longer and several more discharge cycles occur in an orbiter mission. Also, because orbit insertion and orbit trim maneuvers may occur within 24 hours of each other, charge rates are almost twice as large as those used on the MM '69 system to fully recharge the battery in the allowed time.

For these reasons, it is necessary to test and verify the adequacy of the MM '69 battery for orbiter missions.

Other silver-zinc cells, specifically designed for Mars orbiter missions, have been built and successfully tested at GE in accordance with orbiter mission profiles. The cells closely approximate the capacity and physical characteristics of the Mariner battery cells. Such cells might be considered as a backup to the prime selection.

4.7.7 POWER DISTRIBUTION -- MODULE 4A15

The MM '69 power distribution module provides the functions shown in Figure 4.7-14.

The necessary changes to this module for use in the shunt regulated system are summarized below:

- Remove battery boost relay drive circuit
- Modify the zener reference to operate from a regulated bus of 36.7 vdc

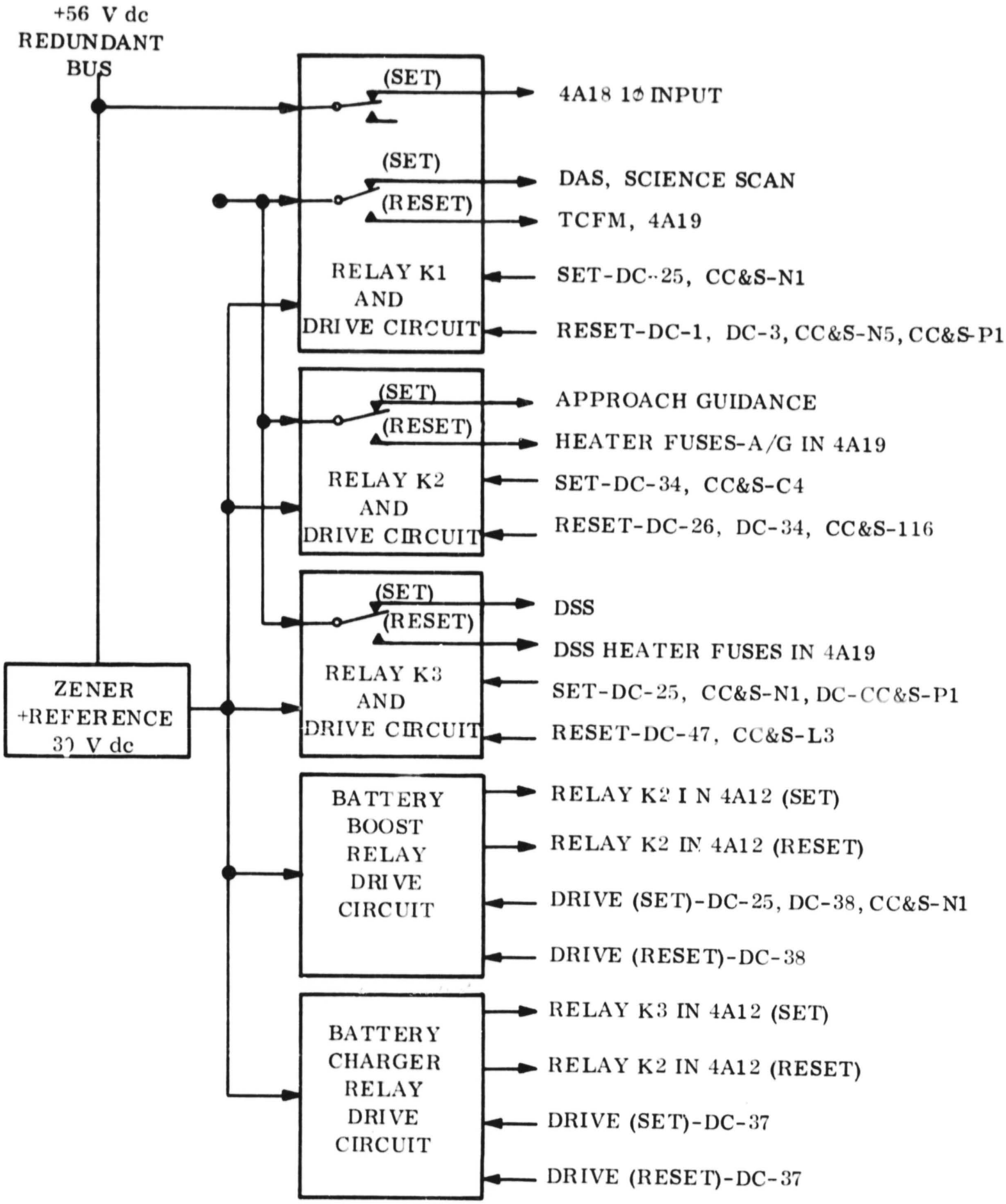


Figure 4.7-14. Power Distribution Subassembly 4A15 Block Diagram

Other possible power control changes may result from system level considerations, number of relays controlling science, etc., as discussed in Section 4.5.

4.7.8 2.4 kHz MAIN INVERTER -- MODULE 4A16

The main inverter generates the spacecraft distribution voltage (50 vrms, square wave, 2.4 kHz) and operates from the regulated input 56-volt bus. The inverter is rated at 200 watts continuous with a minimum power factor of 0.95 lagging. The minimum conversion efficiency is 86 percent at 150 watts output. The output frequency is 2.4 kHz $\pm$ 0.01 percent. In the event of a clock failure, the inverter will free run at 2.8 kHz $\pm$5 percent. The MM '69 inverter circuit block diagram is shown in Figure 4.7-15. The inverter contains power switching transistors in a push-pull transformer configuration. The power switch frequency is controlled by a crystal oscillator for frequency accuracy and stability. The countdown chain converts the crystal frequency to 2.4 kHz, which is used to sync the power switch drive circuits. In the event of crystal failure, the inverter has free run capability at a frequency significantly different from the normal frequency so that a frequency shift may be easily detected.

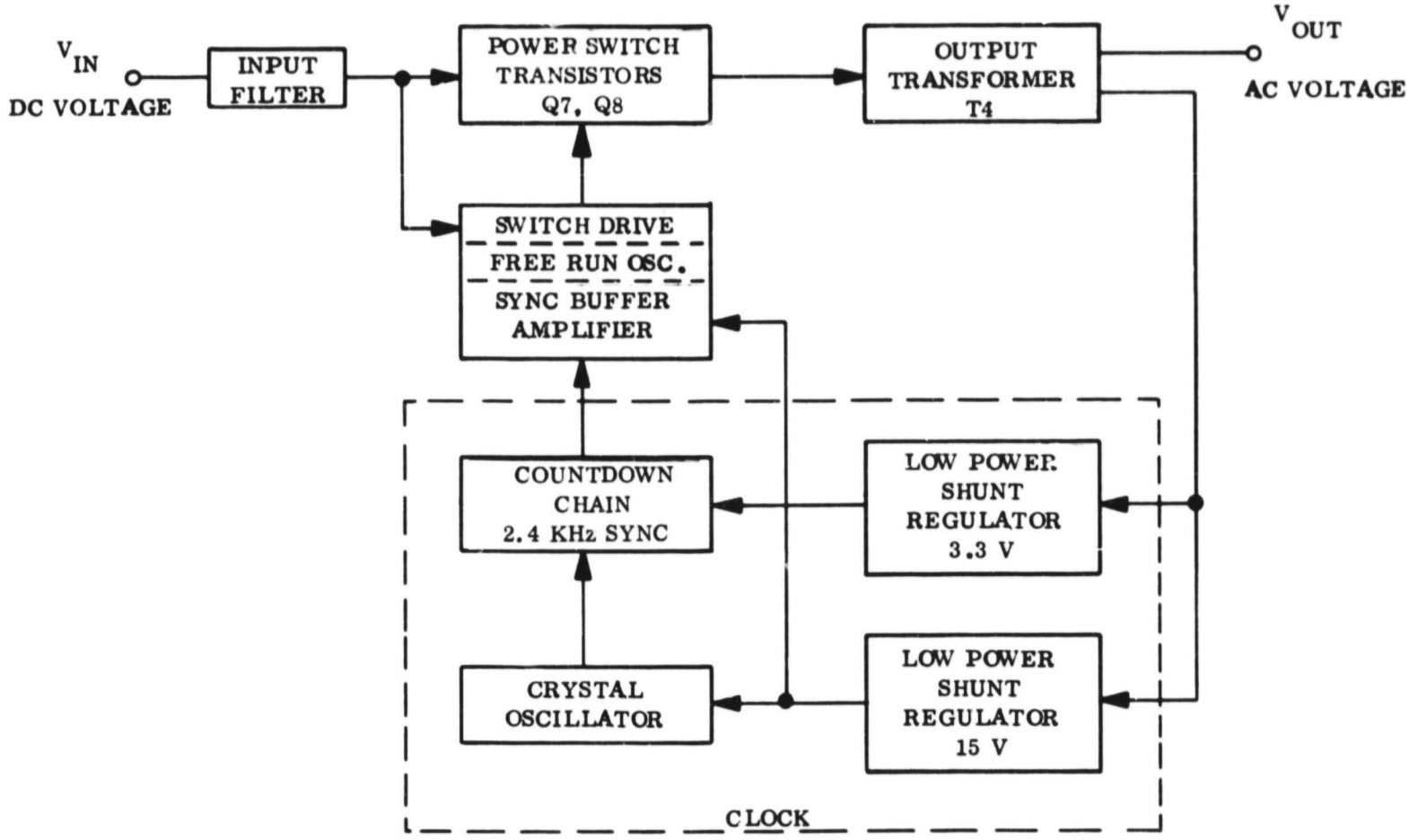


Figure 4.7-15. 2.4 kHz Inverter Block Diagram

The necessary changes to the inverter module for use in the shunt regulated system are summarized below:

- Decrease input voltage from 56 to 37.5 volts
- Increase output power from 200 to 220 watts -- based on load profile
- Add overload transient capability of 150 percent for 0.1 seconds -- based on load fault protection analysis of Section 5.1.5
- Add overload protection -- protect inverter regardless of load fault
- Provide modifications for synchronizing power at no less than 2.16 kHz -- this relates to protection of the 400 Hz inverter discussed in Sections 4.4.1 and 4.7.10

The input voltage change and power increase have little effect on inverter size and performance. The addition of overload transient capability may require additional power transistor drive which may reduce the inverter efficiency by about one percent; however, the inverter size will not be affected since the time duration of the overload is short and associated thermal dissipation is small (see Figure 4.7-16).

Overload protection requires the addition of an output current transformer, magnetic amplifier, control circuits, and diodes for the resultant reactive loads. These additions are shown in Figure 4.7-17. The overload characteristics is shown in Figure 4.7-17, Curve A. The control characteristic (Curve B) shows the normal reset current through MA-1 for all load conditions. Under normal loads MA-1 is always reset. When MA-1 saturates, the ON power transistor is switched off. During overloads greater than 1.5 times the rated load current, the load current controls the duty cycle of the power transistors reducing the output voltage and output current to match the load fault impedance.

During overloads greater than 1.5 times the rating, the output voltage decreases and the clock frequency could change in the existing arrangement, since the clock receives power from the output of the inverter. Hence, a load fault during 400 Hz inverter operation could cause the 400 Hz inverter sync frequency or drive to decrease to a dangerously low level where

NOTE 1. REFER TO JPL DRAWING 10012721, SCHEMATIC DIAGRAM MAIN INVERTER 4A16.

2. PIECE PARTS WITHIN DASHED LINES ARE ADDED FOR OVERLOAD PROTECTION

3. OVERLOAD PROTECTION CHARACTERISTIC IS SHOWN IN FIGURE 4.7-17

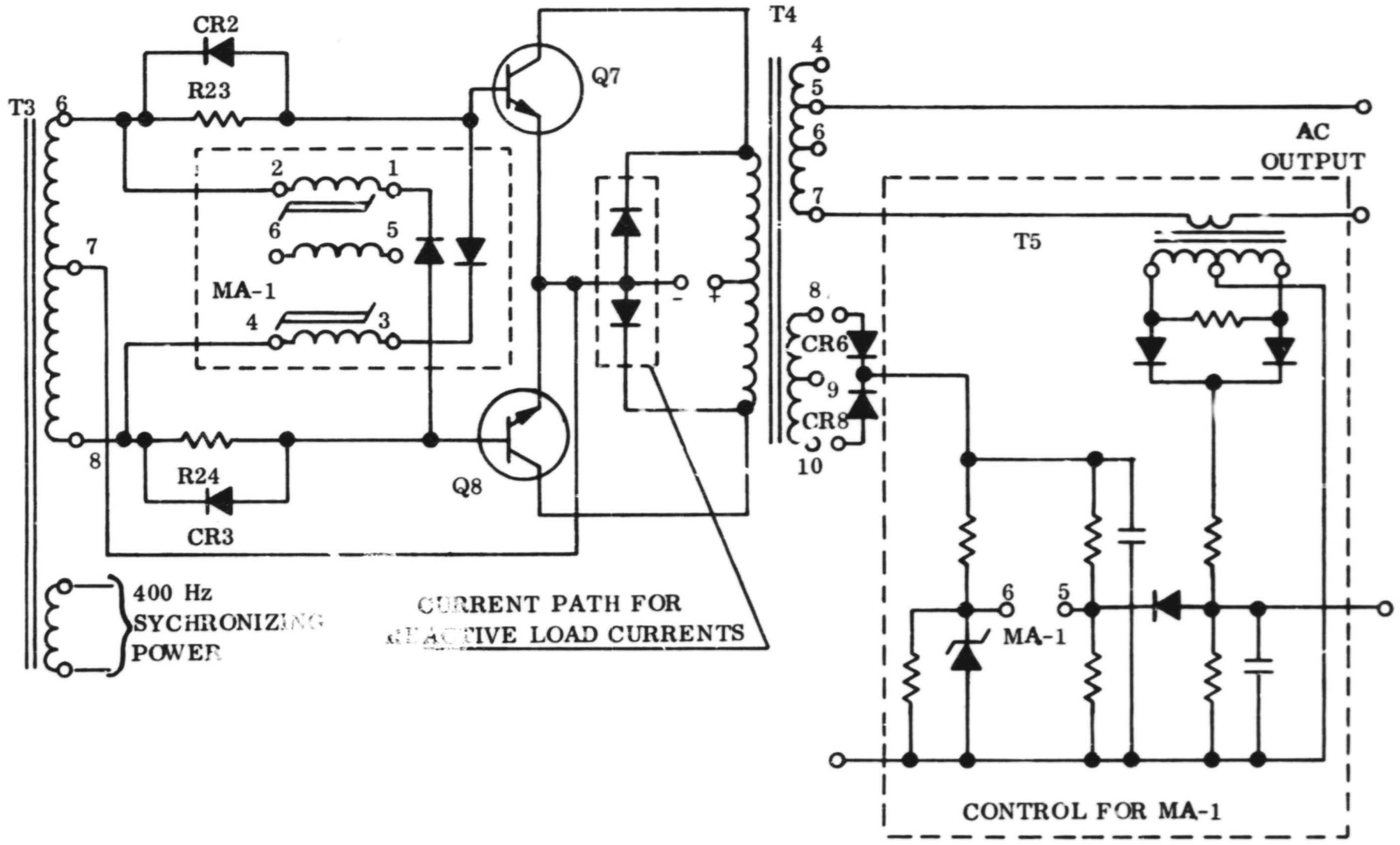
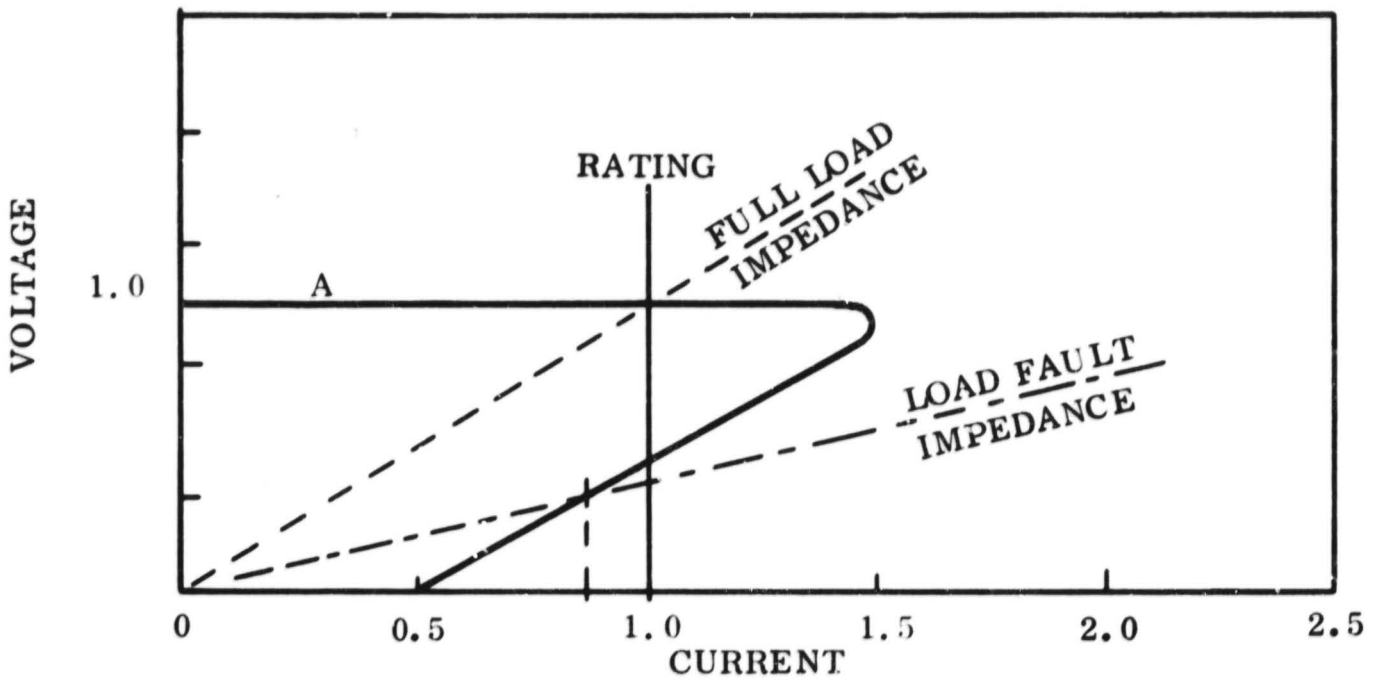
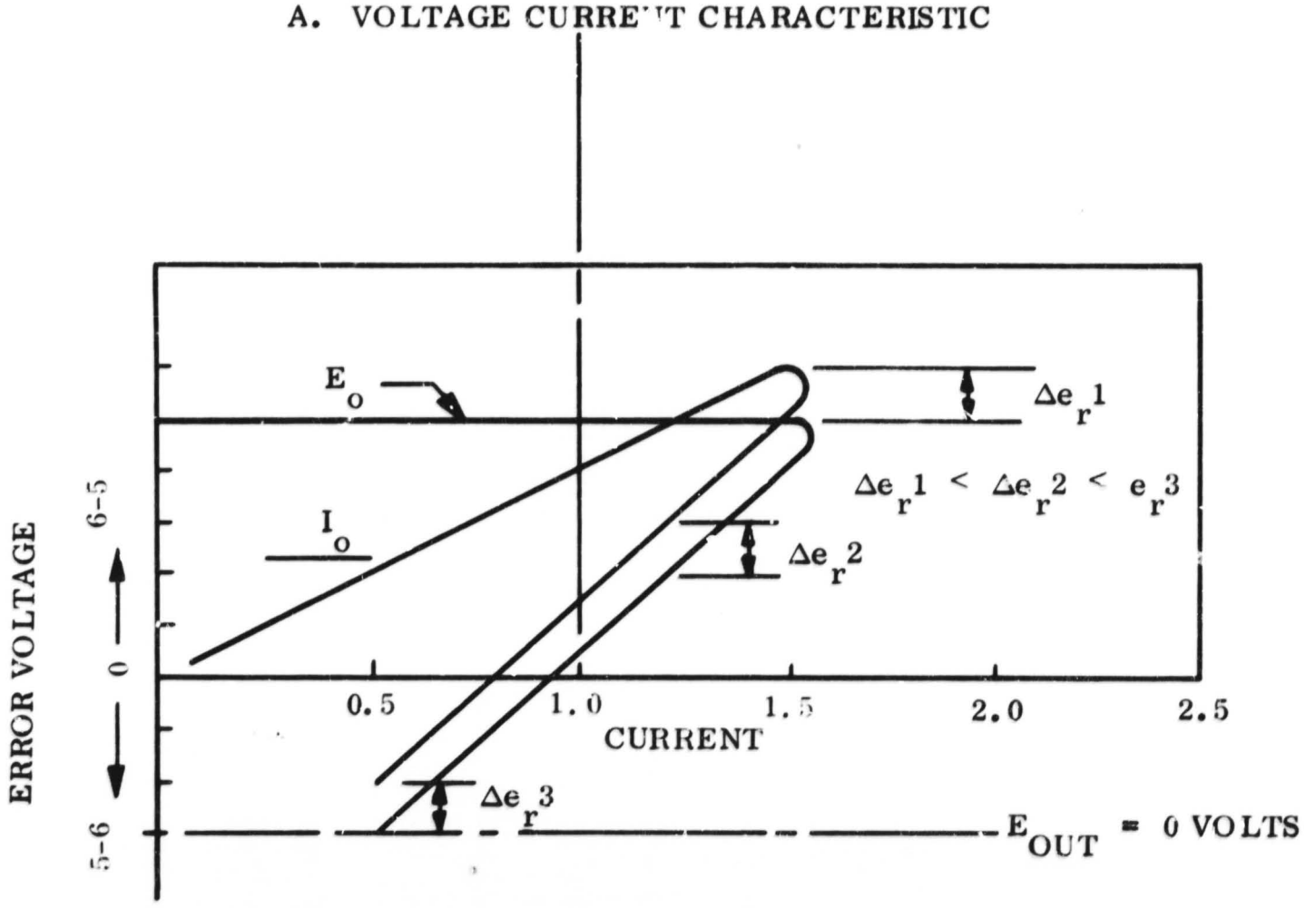


Figure 4.7-16. Inverter Overload Protection



A. VOLTAGE CURRENT CHARACTERISTIC



B. CONTROL CHARACTERISTIC FOR MA-1

Figure 4.7-17. Overload Protection Characteristics

damage to the 400 Hz inverter could occur. Therefore, the requirement that the synchronizing power for the 400 Hz inverters be no less than 2.16 kHz and at constant amplitude is added. This suggests that the crystal oscillator should operate from the regulated input voltage and not the inverter output. Since the crystal oscillator operates with a 15-volt input, a low power series dissipator regulator would be applicable. Figure 4.7-16 also shows where the sync power for the 400 Hz inverters could be derived.

These changes result in an increase in weight (0.13 lb) primarily due to the overload protection magnetic components.

4.7.9 2.4 kHz STANDBY INVERTER -- MODULE 4A17

The MM '69 standby inverter is similar to the main inverter, except that the free run frequency is 2.4 kHz ±5 percent.

The changes in the standby inverter for use in the shunt regulated system are the same as identified for the main inverter in Section 4.7.8, except for the free run frequency noted above.

4.7.10 SINGLE AND THREE PHASE 400 Hz INVERTER -- MODULE 4A18

The MM'69 400 Hz inverter contains a single phase section for science loads, a three phase section for gyro loads, and a 2.4 kHz to 400 Hz synchronizer as shown on Figure 4.7-18. The single and three phase sections derive power from the 56 vdc regulated bus and are only energized when they must supply power to their particular loads. The synchronizer operates continuously.

The necessary change to the 400 Hz inverter for use in the shunt regulated system is noted below:

- Modify the single and three phase sections to operate from an input regulated bus of 36.7 vdc

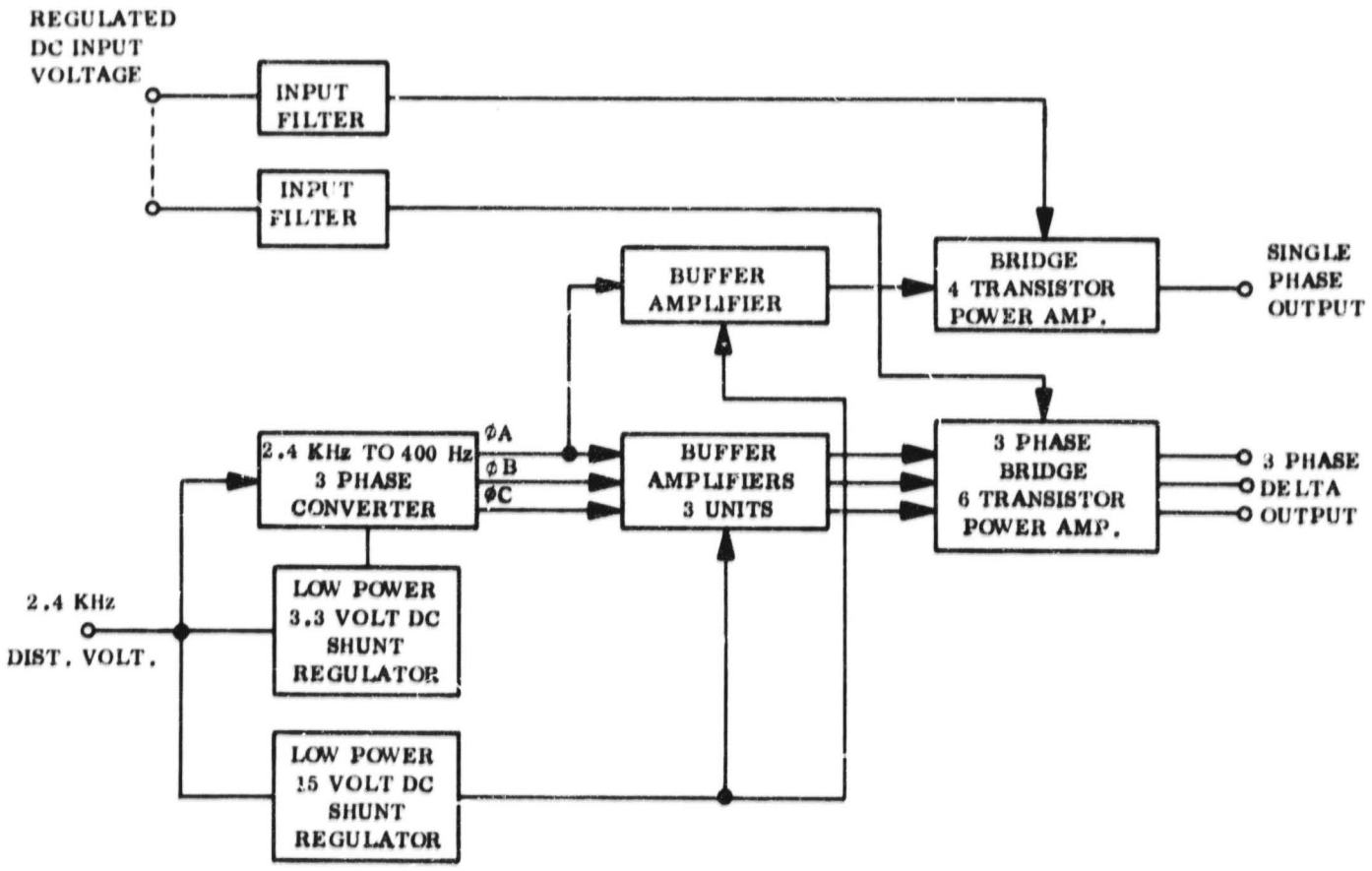


Figure 4.7-18. MM '69 400 Hz Inverter (4A18)

Consideration might also be given to operating the synchronizer only when the single and three phase power sections are required to supply power as a possible means for improving reliability. To obtain this possible improvement, both the synchronizer and power sections must be activated simultaneously. This change does not appear to be difficult; however, testing would be required to substantiate this belief.

Another possible change is to consider the use of 2.4 kHz input power to the synchronizer taken from a preamplifier stage of the 2.4 kHz inverter at a lower voltage. This change would reduce possible damage to the 400 Hz inverter in the event of overload conditions at the output of the 2.4 kHz inverter. Such overload conditions could result in the loss of 2.4 kHz to 400 Hz synchronization or loss of drive power to the 400 Hz power amplifiers with the possibility of their damage.

4.7.11 HEATER AND DC POWER DISTRIBUTION -- MODULE 4A19

The MM'69 heater and dc power distribution module contains power control, load protection, and telemetry sensor functions as shown on Figure 4.7-1 relative to the distribution of raw dc power.

Possible changes in this module for use in the shunt regulated system will depend on system level considerations as discussed in Section 4.5.

4.8 WEIGHT AND PACKAGING SUMMARY

For estimating power system weight, the present MM'69 power system weight summary was used as a reference.* It is recognized that since the power requirements have not changed greatly, the use of general power conditioning equipment power-weight data curves are not valid to accurately identify power system weight. Therefore, the actual functional component weight and piece part details were used to identify the weight change to each functional component. Table 4.8-1 and 4.8-2 provide a weight summary and tabulate initial weight and identify the change and associated weight changes. In all cases the module size (overall dimensions) have not changed. A net increase of 0.3 pound has been identified for the shunt system.

4.9 INTERFACES

Recommended telemetry and command requirements for the prescribed shunt system are discussed below.

4.9.1 TELEMETRY

Table 4.9-1 lists the recommended telemetry points along with appropriate measurement ranges, priority ranking, and suggested sampling rates which conform to the format of MM'69 telemetry equipment. A general rationale for these selections is presented below.

---

* M69-3-250A, Functional Requirements, Mariner Mars 1969 Flight Equipment and Weight List.

Table 4.8-1. Assembly Unit Weight Changes

Module No.	Module Description	Weight (lb)	Function Change	Weight Change (lb)	Δ (lb)	Final Weight (lb)
4A1, 3, 5, 7	Array	12.50	Remove zeners-add transistors Add heat sink for transistors Add test circuit Harness revisions	-5.23 +5.46	+0.20	12.55/panel
4A8	Power Source Logic	8.43	Add Earth-Mars mode relay	+0.125	+0.125	8.55
4A9/10	Boost Main Regulator	6.12	Modify transformer (lower output voltage) Modify output filter or freq of operation Add array/boost isolation diode	-0.062 +0.066	≈ 0	6.12/regulator
4A11	Power Control	3.00	Modify failure detector (Current Monitor) Remove CR8 (Transformer)	+0.225 -0.067	+0.158	3.16
4A12	Battery Charger	2.31	Remove shaze booster Add shunt amplifiers + Relay	-0.925 +0.482	-0.443	1.87
4A15	Power Distribution	2.00	------	----	----	2.00
4A16/17	Main Inverter 2.4 kHz	2.94	Modify transformer (lower input voltage) Overload protection (controls + relay) Modify input choice	-0.068 +0.334	+0.266	3.07/inverter
4A18	400 Hz Inverter 3 Φ, 1Φ	3.87	Modify transformers (lower input volt) Modify drive circuits Modify input chokes	---- ----	---- ----	3.87
4A19	Heater and DC Power Distribution	2.00		----	----	2.00

Table 4.8-2. Weight Summary

Module Description	MM'69		Shunt System		Changes	
					(-)	(+)
Solar Array	12.50	50.00	12.55	50.20	----	0.20
Boost Regulator	6.12	12.24	6.12	12.24	----	----
Inverter, 2.4 kHz	2.94	5.88	3.07	6.14	----	0.26
Battery Charger	2.31	2.31	1.87	1.87	0.44	----
Power Control	3.00	3.00	3.16	3.16	----	0.16
400 Hz Inverter	3.87	3.87	3.87	3.87	----	----
Power Source Logic	8.43	8.43	8.55	8.55	----	0.12
Power Distribution	2.00	2.00	2.00	2.00	----	----
Heater dc Power Dist.	2.00	2.00	2.00	2.00	----	----
Battery	30.80	30.80	30.80	30.80	----	----
Total		120.53		120.83	0.44	0.74

Table 4.9-1. Telemetry List

Item No.	Parameter *	Measurement	Purpose	Parameter Range	Priority Ranking **	Sampling Rate ***
1	I	Array Current	Electrical status, array performance	0-12 amps	2	M
2	I	Raw Load Current	Electrical status	0-5 amps	2	M
3	I	Battery Discharge Current	Electrical status, discharge state	0-20 amps	1	M
4	I	Battery Charge Current	Electrical status, charge state	0-3 amps	1	M
5	I	Boost Output Current	Electrical status	0-15 amps	2	M
6	I	Inverter Output Current	Electrical status	0-5 amps	2	M
7	I	400 Hz Input Current	Electrical status	0-1 amps	2	M
8	E	Shunt Amplifier Voltage	Electrical status	0-40 volts	3	L
9	E	Raw Bus Voltage	Electrical status	20-42 volts	1	H
10	E	Reg Bus Voltage	Electrical status	35-40 volts	3	M
11	E	Battery Voltage	Electrical status	20-40 volts	2	M
12	E	2.4 kHz Bus Voltage	Electrical status	47-53 volts	2	M
13	T	Array Temperature	Long-term array temperature history	0 to +180°F	2	LL
14	T	Array Temperature	Transient array temperature history	-250 to +180°F	4	L
15	S	Earth/Mars mode	Command verification	State	1	EM
16	S	Main/Standby Switch	Failure diagnosis	State	4	EM
17	S	Charge Regulator Switch	Command verification	State	2	EM
18	I	Shunt Current	Array V-I characteristic	0-1.5 amps	4	LL
19	I	Array Section Current	Array V-I characteristic	0-0.5 amps	4	LL
20	E	Shunt Voltage	Array V-I characteristic	0-20 volts	4	LL
21	T	Battery Temperature	Indication of overcharge	0-120°F	2	LL

*I = Current
E = Voltage
T = Temperature
S = State

**Priority Ranking
1 = High
2 = Intermediate High
3 = Intermediate Low
4 = Low

***

Sampling Rate	Sampling Period	
	Fast-33 1/3 bps	Slow-8 1/3 bps
H = High	4.2 seconds	16.8 seconds
M = Medium	42	168
L = Low	420	1680
LL = Low-Low	840	3360

EM = Event Monitor

a. Electrical Status. Items 1 through 12 permit the determination of voltage and current levels at all significant points in the system, either through the direct measurements themselves, or by derived calculation. Electrical status monitors are generally ranked in the "intermediate high" category, except for the following:

(1) Items 3 and 4 are given a high rating since battery status strongly influences mission operations and contingency planning. Subsequent to Orbit Insertion, for example, the battery watt-hour reserve must be known before Orbit Trim maneuvers are attempted. This can be deduced from ground based calculations using the information from Items 3 and 4.

(2) Item 8 is ranked somewhat lower since it can be inferred from Item 18.

(3) Item 9 is given the highest ranking since it is the most important measurement indicating system viability or abnormal spacecraft operation; e.g., loss of solar reference during cruise is implied by a drop in E_9 to battery discharge levels indicating a need for contingency actions.

(4) Item 10 is given an intermediate low rating since its value is implied by Item 12.

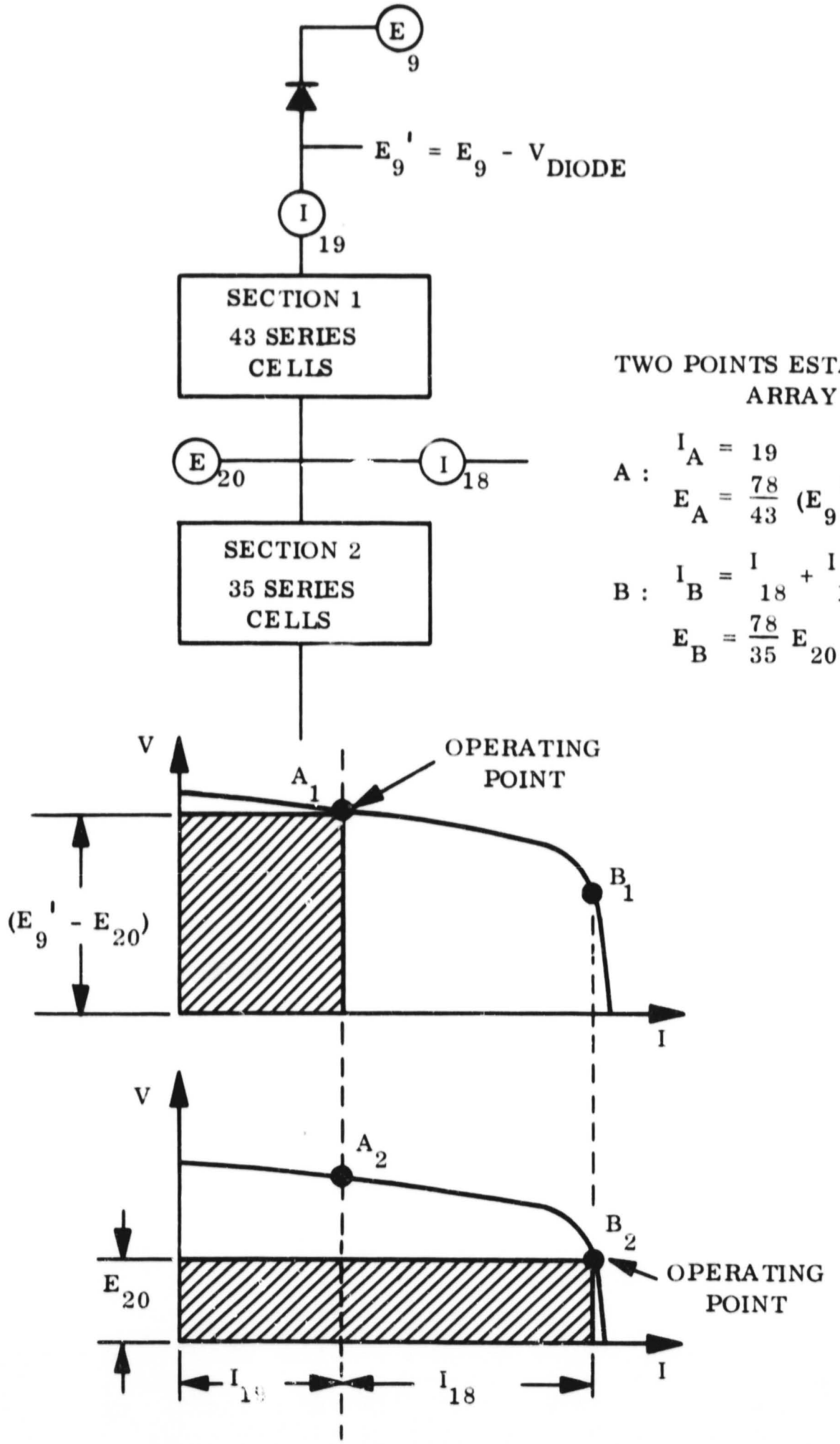
b. Array Performance. Items 13, 14, 18, 19 and 20 augment array performance information derived from Items 1 and 9:

(1) The limited temperature range of Item 13 permits a more accurate determination of array temperature performance.

(2) The wide temperature range of Item 14 will permit an examination of transient array temperature conditions during maneuver operations.

(3) Items 18, 19 and 20 are given low priority and are associated with determining solar array V-I characteristics. The use of a partial shunt regulation system permits the determination of several points on the V-I characteristic as described in Figure 4.9-1.

(4) Concerning Item 1, it was decided to measure overall array current rather than separate panel currents. The rationale for this is that it is assumed that event monitors will indicate whether or not the panels are properly deployed (these telemetry requirements are assumed to exist elsewhere). Although four separate measurements permit the identification of discrete array failures, this can also be determined with an overall current measurement in conjunction with the current measurement of one array section (Item 19). If the overall current is not about 24 times the section current, it may be surmised that some sections have failed and contingencies can be executed on that basis.



TWO POINTS ESTABLISHED ON TOTAL ARRAY SECTION:

A : $I_A = 19$

$E_A = \frac{78}{43} (E_9' = E_{20})$

B : $I_B = I_{18} + I_{19}$

$E_B = \frac{78}{35} E_{20}$

Figure 4.9-1. Two Point V-I Determination by Telemetry Data

c. State Conditions. Items 15, 16 and 17 are related to subsystem status. A knowledge of Item 15 is important to avoid potential array/battery load sharing problems. Item 16 indicates whether a fault has occurred with transferral to the redundant boost/inverter/amplifier group. It is given low priority since there is no recourse action possible.

d. Battery Performance. Item 21 provides battery temperature information, which along with Items 3, 4, and 11, permit overall battery evaluation.

4.9.2 COMMAND

Table 4.9-2 lists the commands and other stimuli for controlling the power system. These are also designated on the block diagram, Figure 4.4-1.

4.10 TEST APPROACH

In comparing the MM'69 system and the selected shunt system, the main difference in test procedures results from the use of the shunt regulator. In the MM'69 system, control is provided at the downstream side of the solar array, while in the implementation of the shunt system, control is provided within the solar array itself. This difference has its greatest impact during test sequences in which the solar array is electrically simulated. Such sequences will occur during subsystem and system tests when it may be inconvenient to conduct tests with illuminated solar arrays and during on-pad checkout tests. Equipment identification for these cases are discussed below.

4.10.1 SUBSYSTEM/SYSTEM TESTS WITH ARRAY SIMULATION

Test equipment identification for these cases is shown on Figure 4.10-1 and consists of the following:

- Upper array simulator which has adjustability to reproduce the upper array V-I characteristics over its range of variability
- Lower array simulator with similar adjustability
- Array shunt simulator whose shunt transistors receive their base drive signal from the subsystem shunt amplifier

Table 4.9-2. Command and Control Functions

Item No.		Function	Signal Source	Comment No.
Power S/S Functions	F1	Turn on charge regulator	DC	
	F2	Turn off charge regulator	DC	
	F3	Earth mode system operation	DC	
	F4	Mars mode system operation	DC, CC&S	
	F5	Internal Power	OSE	
	F6	External Power	OSE	
	F7	Main boost/inverter	OSE	
	F8	Standby boost/inverter	OSE	
	F9	Switch to standby boost/inverter	Fault Sensor	
Distribution Control	D1	400 Hz - 1ϕ power on	DC, CC&S	
	D2	400 Hz - 1ϕ power off	DC, CC&S	
	D3	Gyro & A/C power on	A/C	
	D4	Power on - typical science load	DC, CC&S	
	D5	Power off - typical science load	DC, CC&S	
	D6	Power off - due to load fault	O.C. trip	
	.	.		
	.	.		
	.	.		
	.	.		
	DX	.		
	DY	.		

Nomenclature:

DC	=	Direct Command
CC&S	=	Computer and Sequencer
OSE	=	Operational Support Equipment
A/C	=	Attitude Control
O.C.	=	Overcurrent

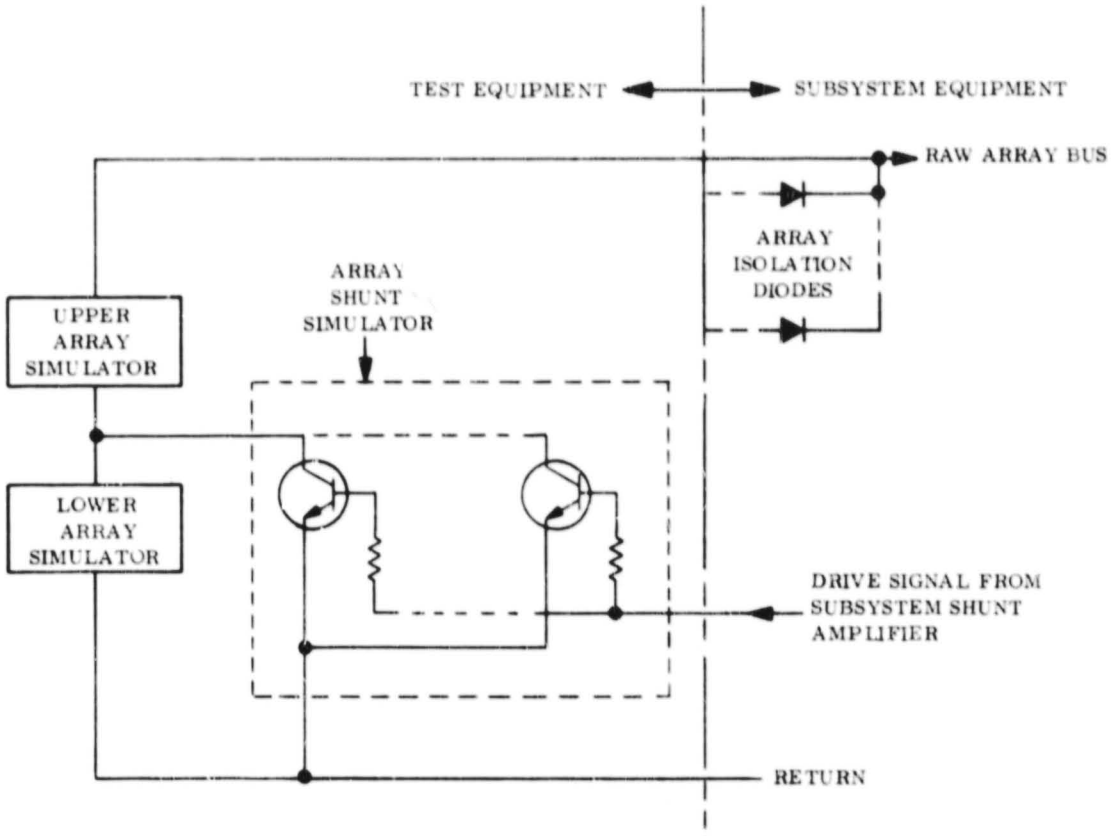


Figure 4.10-1. Subsystem/System Test Configuration

4.10.2 ON-PAD TESTS

The test configuration for checkout of the system with the actual array shunt transistors but with the array nonilluminated is shown on Figure 4.10-2. The array simulators are identical to those described above. To permit the use of a single lower array simulator and at the same time provide isolation for the collector junctions of the shunt transistors, test diodes are installed on the array as indicated. The isolation is desired to prevent a short-circuited transistor from affecting the others. In this test configuration it is important that the lower array simulator voltage be limited to prevent damage to the lower solar array sections. The dark V-I characteristics may be approximated by translating the curves shown on Figure 4.6-9 in the current direction to the point where the short-circuit current is zero. Assuming the array temperature may be as high as 60°C during on-pad checkout, the translated curve indicates negligible current with an applied voltage of 0.3 volts per cell. With 35 series cells in the lower array section, this means the applied open-circuit voltage of the lower

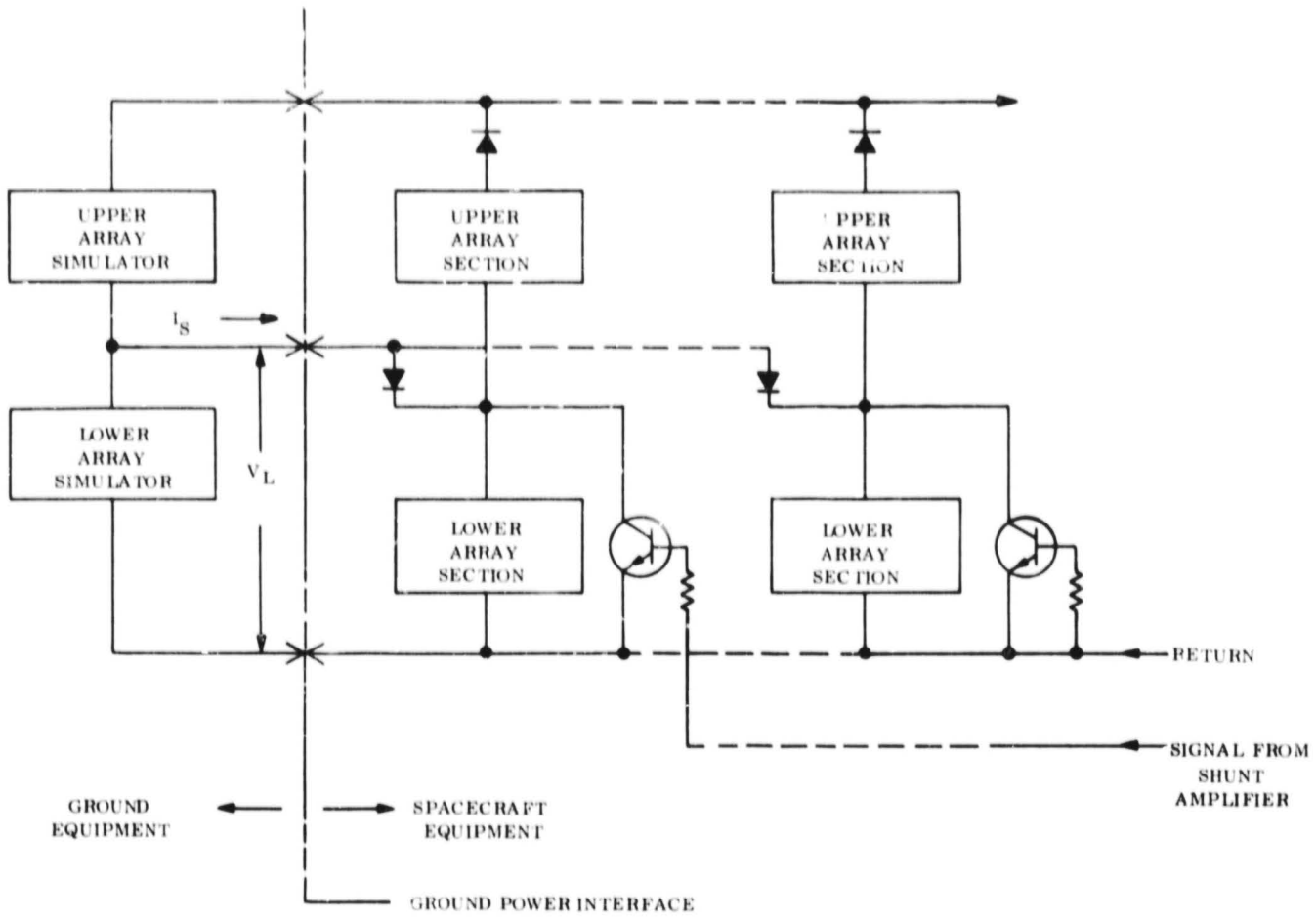


Figure 4.10-2. On-Pad Test Configuration

array simulator should not exceed 10.5 volts. Any higher voltage would result in power dissipation through the solar cells with the possibility of damage. To provide margin in this respect, it is probably best to limit the simulator voltage to 8 volts.

The steps in applying ground power would be as follows:

a. Apply lower array simulator power with its open circuit voltage limited to 8 volts. Adjust the simulator short-circuit current to any desired flight value.

b. Adjust the upper array simulator to the same short-circuit current as in (a) and adjust its voltage until shunt operation is detected. This occurs when I_S current (see Figure 4.10-2) is detected. A further increase in the voltage of the upper array simulator will cause a decrease in the voltage of the lower array simulator and an increase in I_S. When V_L is about 4 volts the shunt is about halfway through its response region which represents an acceptable ground power adjustment for further system testing.

SECTION 5

SUPPORTING ANALYSIS AND TRADE STUDIES

5.1 SYSTEM DESIGN STUDIES

5.1.1 INITIAL BASELINE SYSTEM SELECTION

The following discussion is largely taken verbatim from the Interim Report and describes the early selection of the basic shunt system.

The selection of the shunt system was based on its relatively higher scoring over other candidates when judged against numerous criteria, as discussed in the following sections.

Three principal power system candidates were evaluated in the selection process: (a) a boost regulation system, (b) a series switching (buck) regulation system, and (c) the shunt regulation system. A single representative arrangement of the functional elements was evaluated for each candidate. Only those functions necessary to provide regulated and raw dc power were considered. Although the guidelines listed earlier indicate the distribution of ac power, its impact on candidate evaluation was not considered to be significant since dc/ac conditioning equipment is quite similar for any candidate. Any other features that could be applied with equal advantage to all candidates were also not included, such as improved methods of battery charging.

5.1.1.1 Influence of Solar Array

The variations in solar array characteristics associated with Earth/Mars transfer provided a logical starting point for considering power system candidates. It seemed valid to consider that future Mariner spacecraft would utilize rigid deployed panel solar arrays similar to those used previously.

The variation in voltage-current characteristics is largely independent of the subsystem arrangement of which the solar array is a part. It is therefore possible to use a generalized set of solar array characteristics in examining possible subsystem arrangements.

Figure 5.1.1-1 shows a set of normalized power-voltage curves for a representative Mars spacecraft solar array design based on the use of RCA 1-ohm/cm N/P cells. The effect of possible errors in temperature prediction are also included in the P-V plot for 1.0 AU.

To permit relative assessments of the solar array effect on candidate subsystem arrangements, the P-V curves are normalized and hence independent of specific series-parallel arrangements of the solar cells. Normalization is shown with respect to maximum power and voltage at 1.0 AU and 140° F.

The use of these P-V curves implies that no active means would be used to electrically rearrange solar array sections by switching. The purpose of such switching would be twofold: (a) to add or remove array sections and thus minimize problems of handling excess power, (b) to change the series-parallel solar cell matrix to permit power availability at more favorable voltage levels as a result of large changes in V-I characteristics with sun distance. All of the power system candidates described later are able to cope with these conditions without the necessity for switching; therefore, this possibility was not considered further.

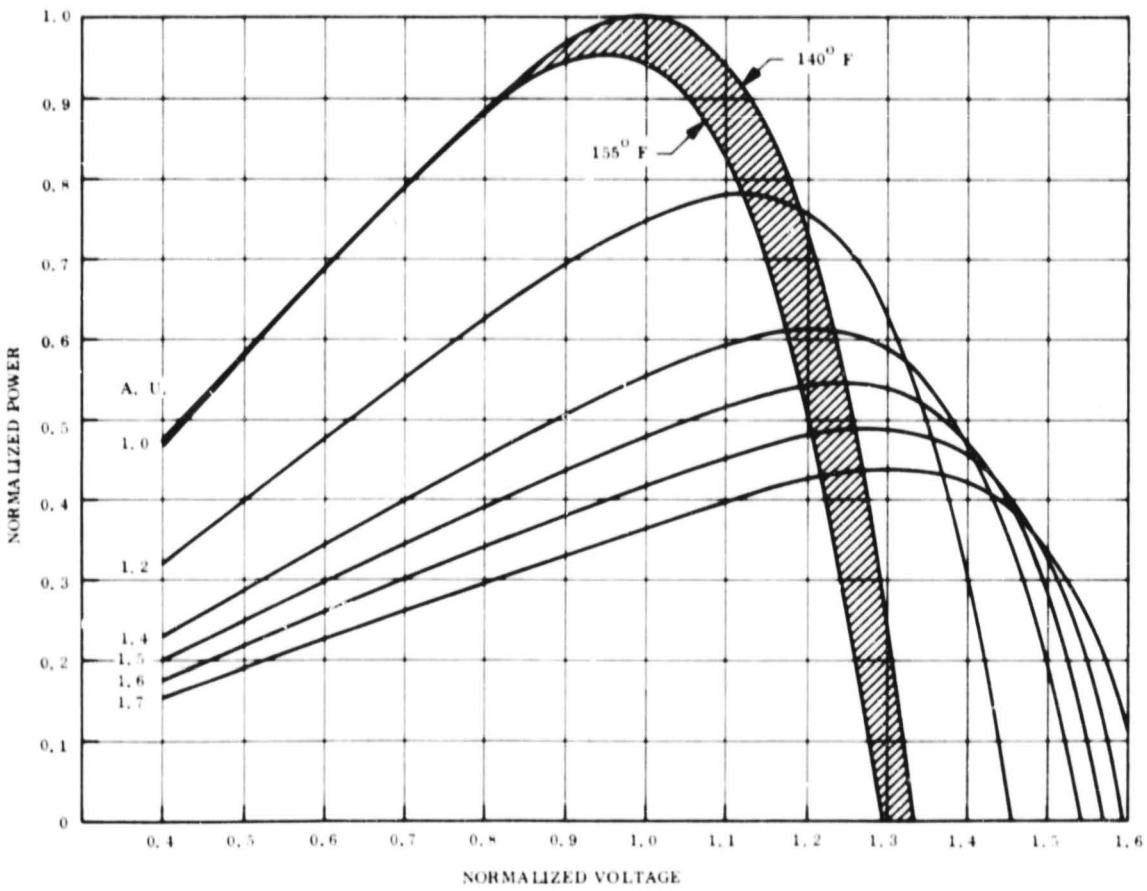


Figure 5.1.1-1. Normalized P-V Solar Array Curves

5.1.1.2 Regulator Efficiency

Regulator efficiency data used in evaluating the candidate systems is shown in Figure 5.1.1-2. The boost regulator data is based on the efficiencies cited in the 1971 load profile information and reflects the performance of the regulator used in the MM '69 power system.

The buck regulator data is based on a GE design rated at 600 watts and 30 vdc which was built as a breadboard and performance tested on previous projects.

The shunt regulator data is based on assuming an efficiency of 98 percent at rated load with 2 percent used for the regulator control electronics. At partial loads, when shunting occurs the same amount of control power is required and all additional control power is considered as part of the required dissipation; therefore, the efficiency is considered constant.

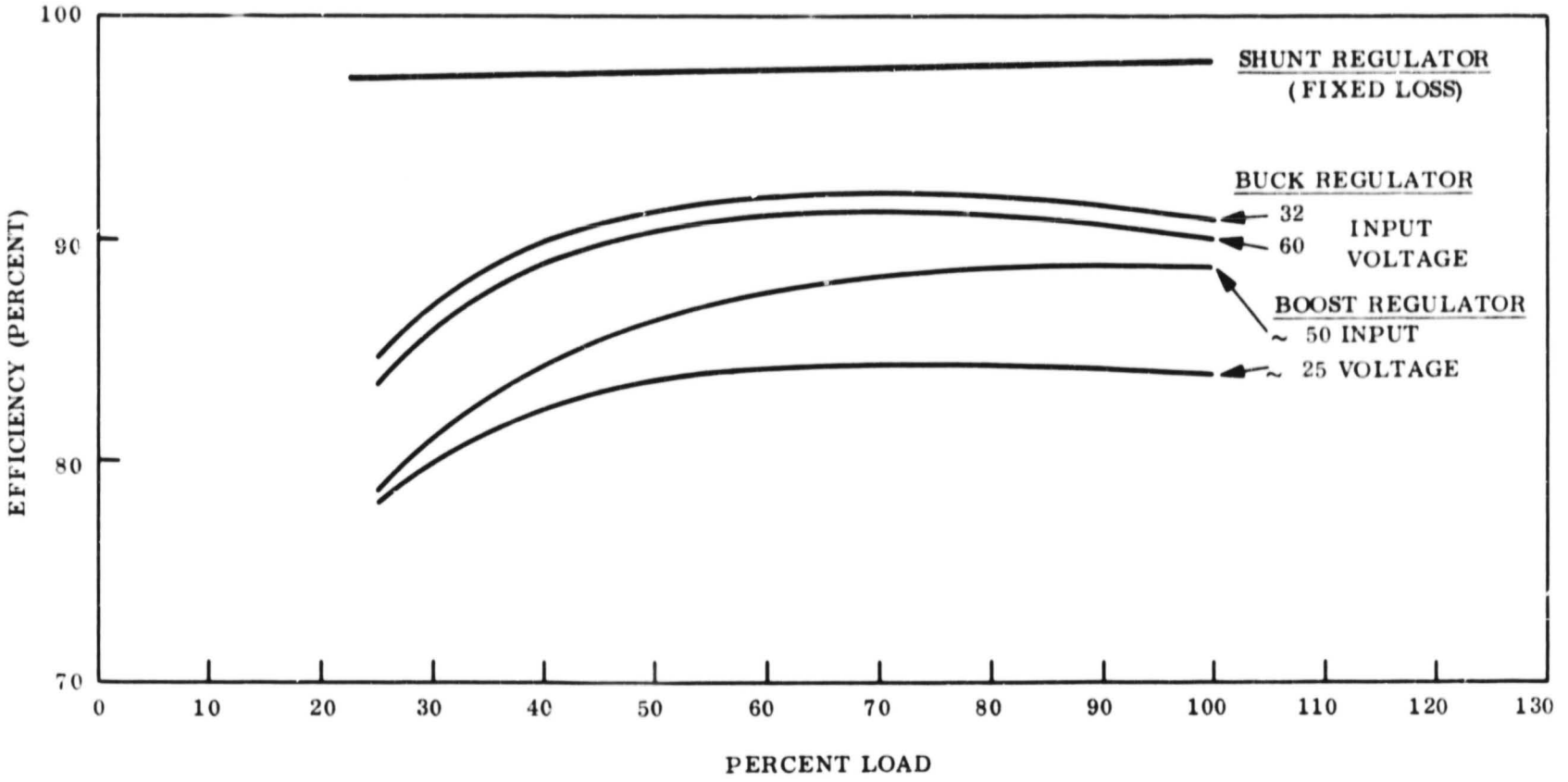


Figure 5.1.1-2. Regulator Efficiency Data

5.1.1.3 Candidate Descriptions

5.1.1.3.1 Boost System

This candidate system is shown on Figure 5.1.1-3a and has the general characteristics of the MM '69 power system.

The boost regulator requires that all input operating voltages be lower than the regulated output voltage. The necessary voltages to meet this condition are shown on Figure 5.1.1-3b with reference to the normalized values for the solar array (Figure 5.1.1-1). The procedure for selecting these levels is described in the following paragraphs.

First, as shown on Figure 5.1.1-1, for an arrival at Mars between 1.4 and 1.6 AU, maximum power is available at a normalized voltage, V_N, of around 1.25. For these particular P-V curves, there is a negligible power difference if V_N is used between 1.2 and 1.3, corresponding to AU distances of 1.4 and 1.6, respectively. An intermediate value of 1.25 appears appropriate under this circumstance.

With array power at Mars drawn at $V_N = 1.25$, it is necessary that the maximum allowable boost input level be set higher than 1.25, with allowance made for zener shunt tolerances. The zener shunt is used to assure that the boost input limit is not exceeded. This could occur as a result of solar array tolerance buildups or upon emergence from solar occultations (i.e., a cold array producing high voltage). With these constraints, V_N for the boost output bus is set at 1.4 with a loose zener tolerance of V_N equal to 1.3-1.4.

A battery charging voltage must be selected which does not interfere with the ability to draw sufficient array power in the near-Earth phase of operations. If, for example, a series dissipative charge regulator is used and its minimum input voltage is set at $V_N = 1.25$, then Figure 5.1.1-1 indicates that insufficient array power is available at 1.0 AU, especially if the solar array operates at 155°F rather than the nominally predicted temperature of 140°F for Mariner panels. By lowering the charger input to $V_N = 1.05$, this problem is avoided and the only penalty is the need for a wider boost input voltage range.

The battery charge to discharge voltage ratio is typically 1.35:1 (for Ag=Zn, V_{charge}=1.94 and $V_{discharge}$=1.44). With a conservative allowance made for a voltage drop through the charge regulator, the total voltage ratio of charger input to battery discharge is about 1.5:1 corresponding to the V_N values of 1.05 and 0.7 shown on Figure 5.1.1-3b.

The limits described above result in a 2:1 variation in raw voltage.

With a boost system designed for these general limits, considerable latitude exists in the design voltage for the solar array. It is estimated that the number of solar cells in series may be varied by about 12 percent without affecting system operation.

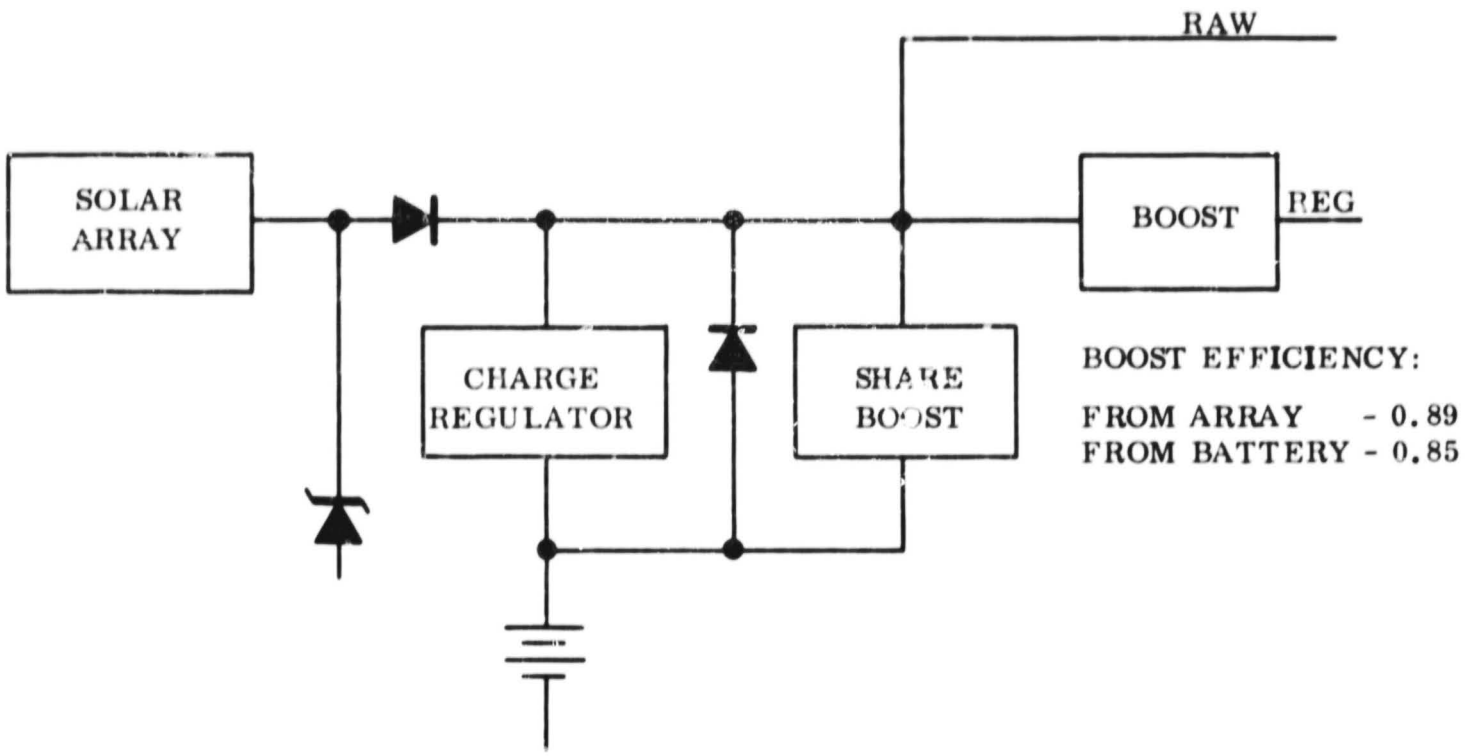
The boost system requires a means for avoiding the simultaneous supply of power from the solar array and battery, although the array might be fully capable of supplying all power. This possibility could occur during certain sequences when the battery clamps the array voltage at a value below its optimum point. A share boost regulator is incorporated to avoid this condition in the manner used on the MM '69 system. Another possibility is to reduce the load momentarily through appropriate sensing logic.

5.1.1.3.2 Series Switching (Buck) System

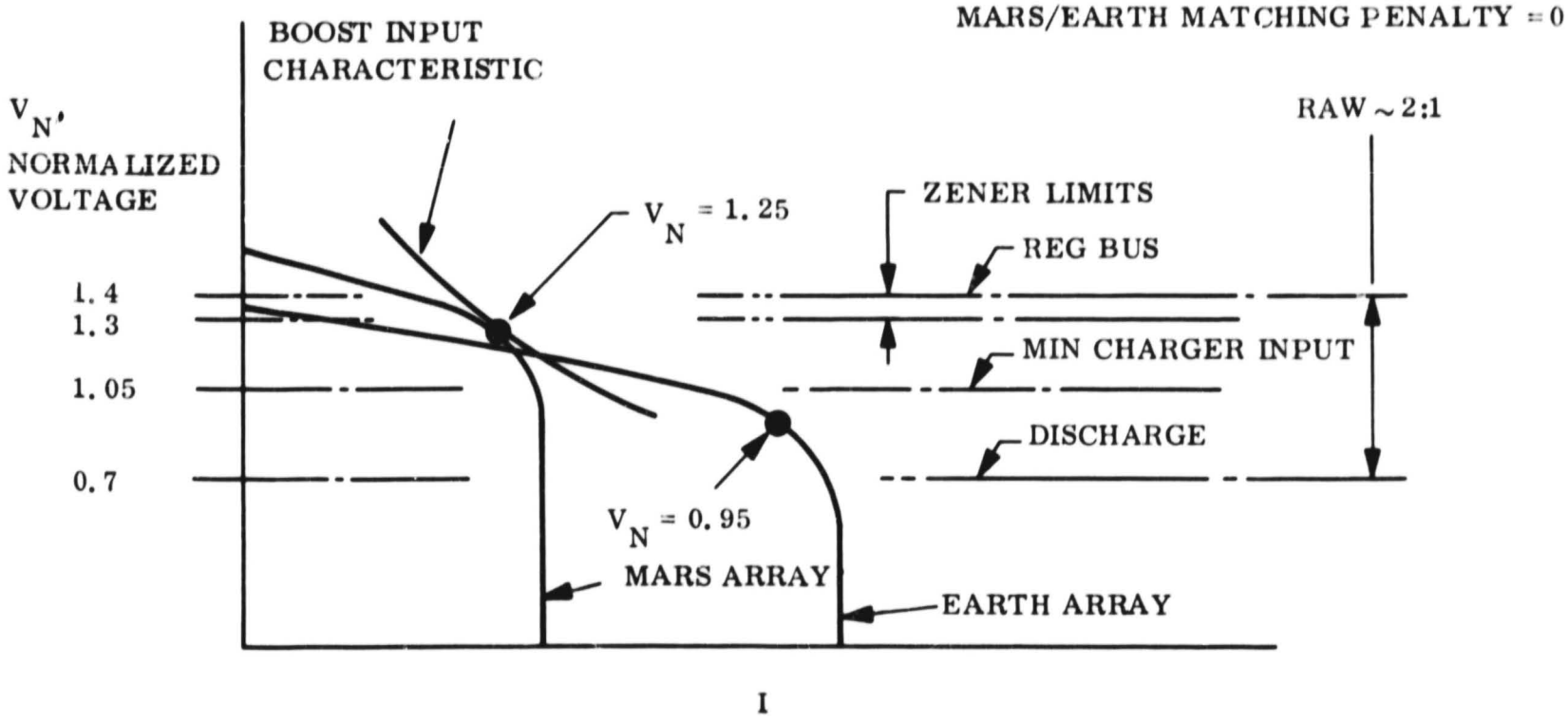
This candidate system is shown on Figure 5.1.1-4a.

The buck regulator requires that all input operating voltages be higher than the regulated output voltage as shown on Figure 5.1.1-4b.

As with the boost system, maximum power at Mars is available at $V_N \approx 1.25$. Sufficient near-Earth power is available at $V_N \approx 1.2$ which sets the minimum charge regulator input voltage. Again, conservatively allowing a 1.5:1 ratio for the relationship of charger input voltage to battery discharge voltage, the latter voltage is set at $V_N = 0.8$. An estimated minimum voltage drop of $V_N = 0.05$ is allocated to the buck regulator to result in a regulated bus level at 0.75.

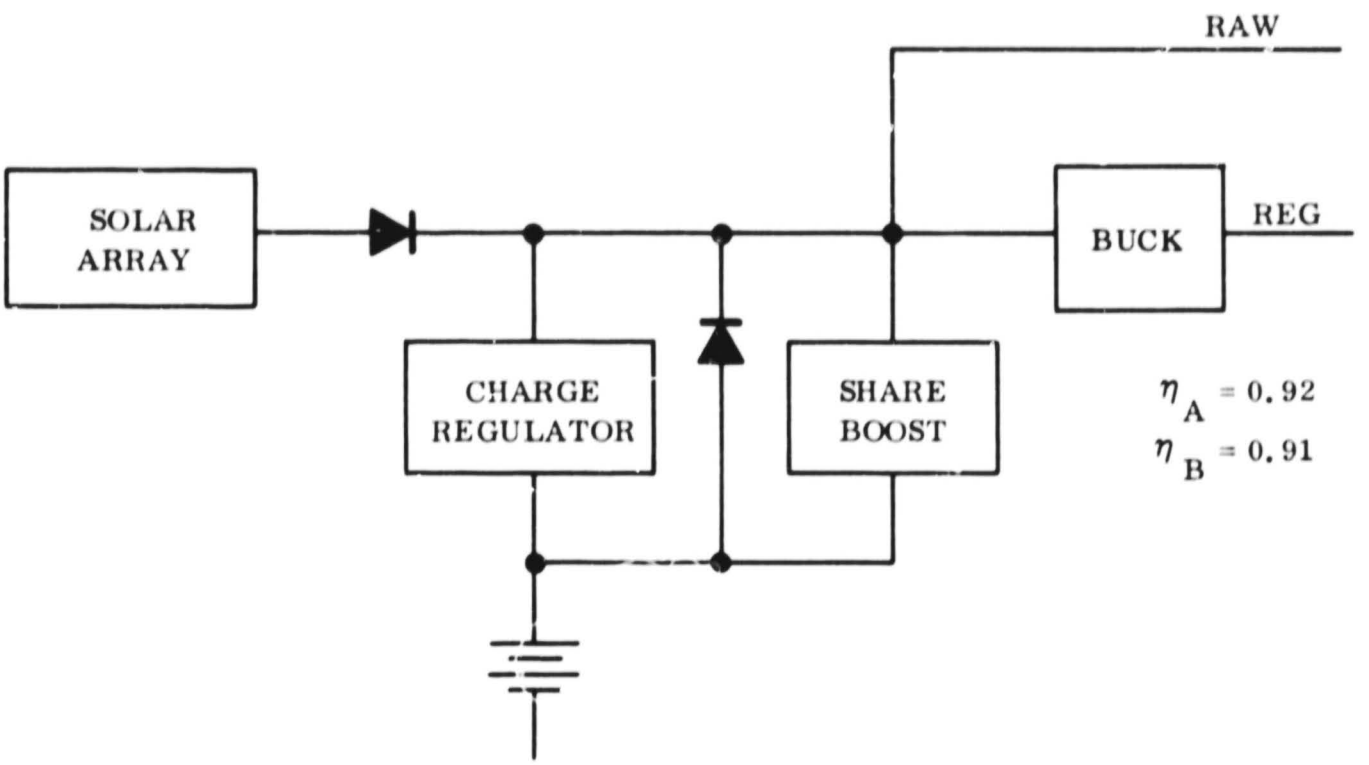


(A)

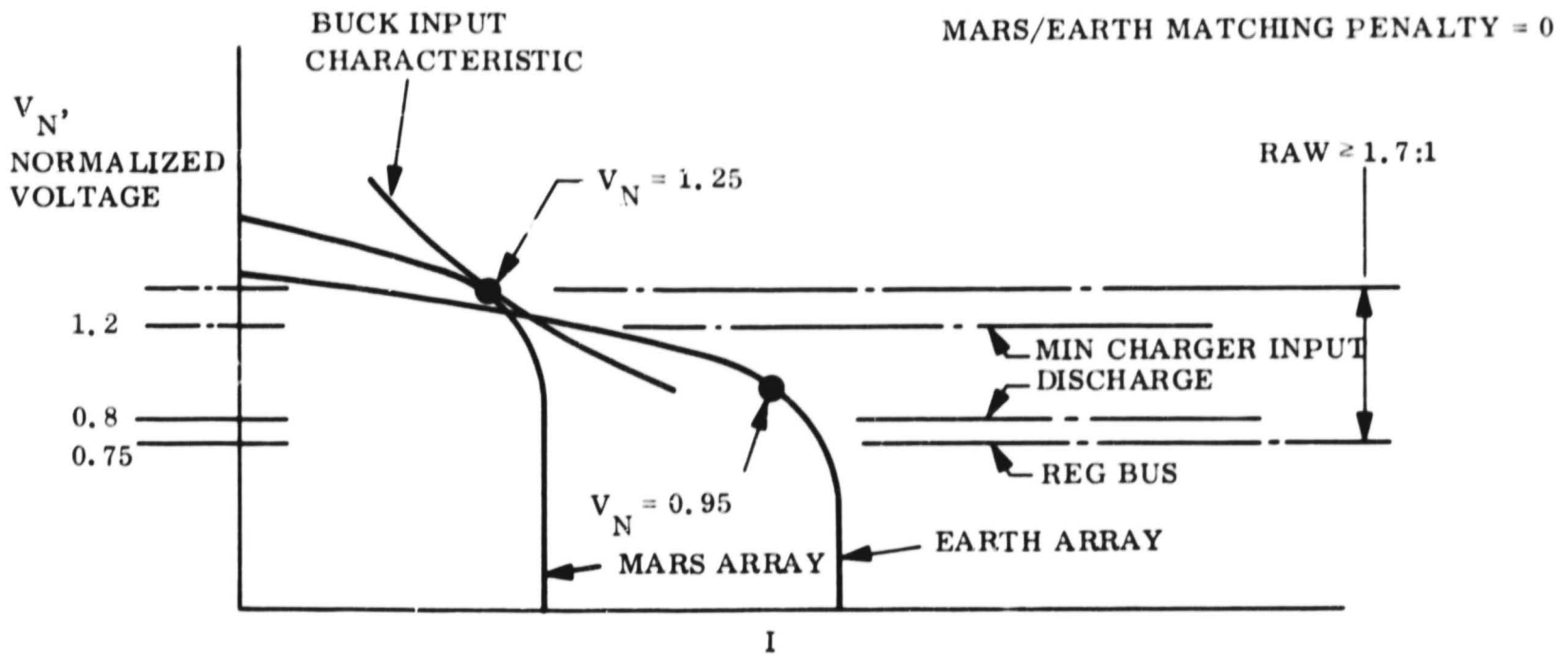


(B)

Figure 5.1.1-3. Boost Candidate



(A)



(B)

Figure 5.1.1-4. Buck Candidate

These established limits result in a 1.7:1 variation in raw voltage.

In this system, an even greater variation in the array design voltage exists. The lower limit is set by conditions which mutually satisfy the near-Earth power demand and the charger input voltage. The higher limit is set by the regulator transistor ratings or the desire to limit the raw power range. A 2:1 input to output range for a buck regulator is realistic which would allow an increase to $V_N = 1.5$ over 1.25. This is equivalent to permitting an array design with 20 percent more cells in series. If the 2:1 range on the regulator was an absolute requirement, it is likely that zener shunts would be required to prevent excess voltage during cold array conditions (emergence from occultations, etc.).

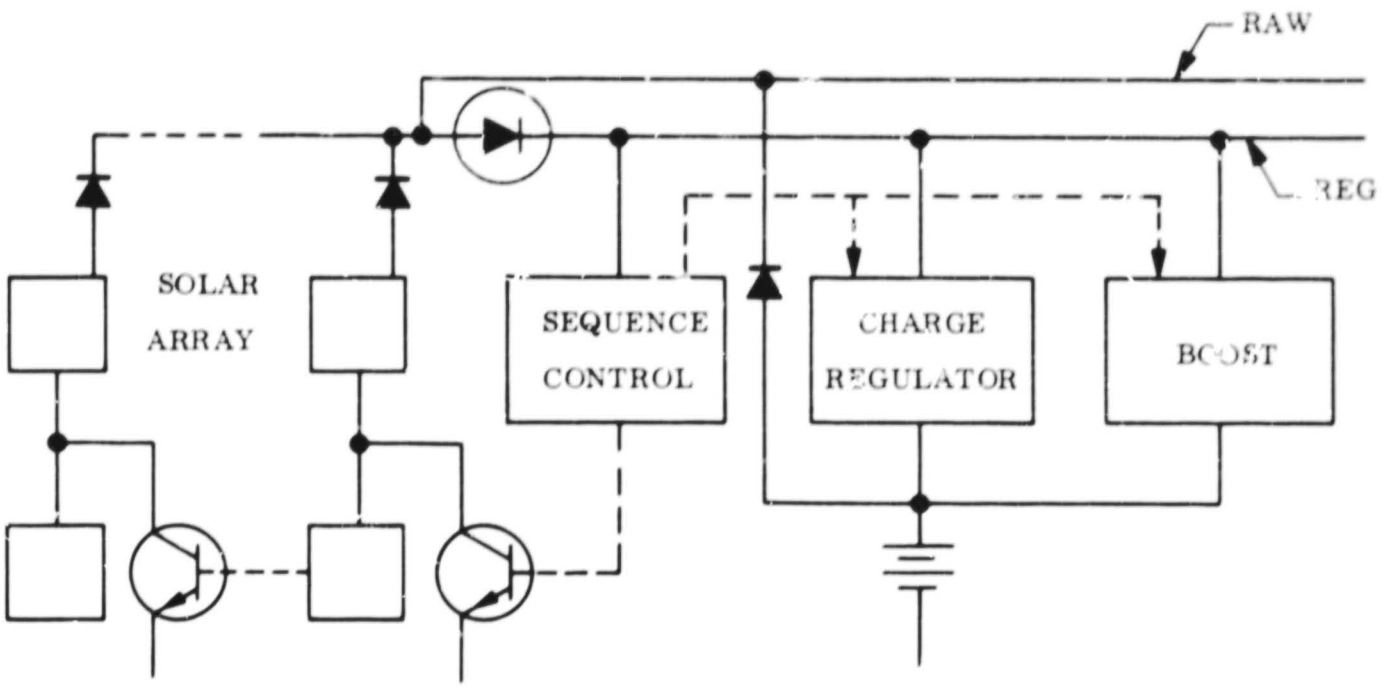
This system also requires a means for avoiding the array/battery load sharing problem.

5.1.1.3.3 Shunt System

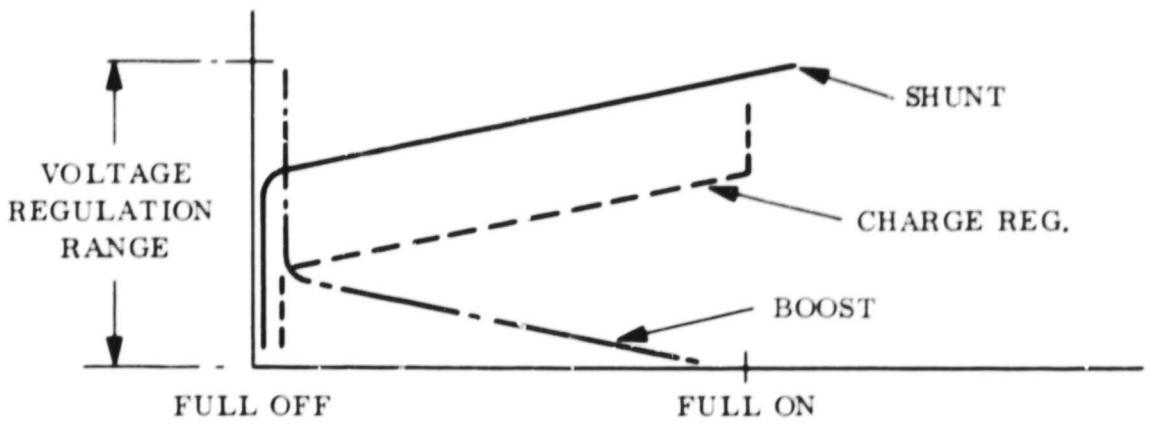
This candidate system is shown on Figure 5.1.1-5

Regulated dc power is drawn directly from the solar array and is controlled by a partial shunt regulator in the form of multiple shunt transistors across separate semi-sections of the solar array.

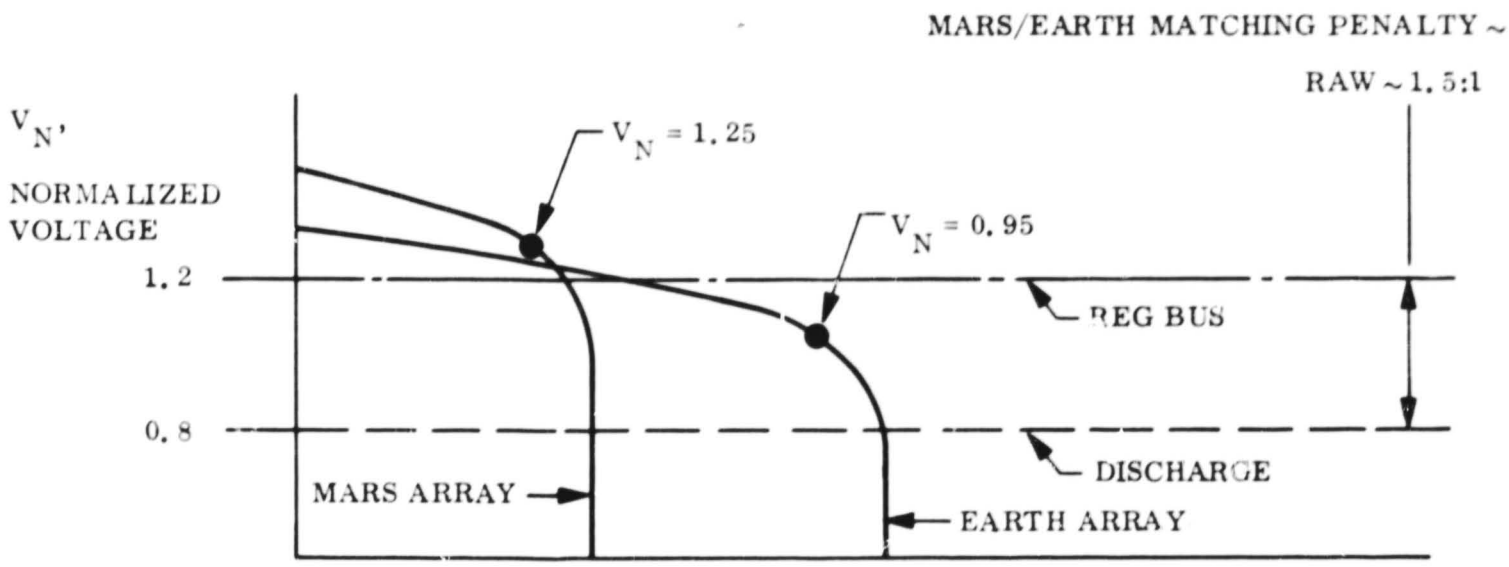
The Sequence Control provides the base drive signal to the shunt transistors and also provides control signals for sequencing operation of the charge regulator and boost regulator. This sequencing is necessary to prevent (a) simultaneous shunt and boost operation, and (b) simultaneous battery charging and boost operation. The method of sequencing is explained more fully on Figure 5.1.1-5b. The Sequence Control establishes shunt, charge regulator, and boost regulator operation as a function of the voltage level within the voltage regulation range. Assume for example that the regulated bus is set at 50 volts ± 1 volt; then the voltage regulation range is 2 volts. Figure 5.1.1-5 indicates that the range is divided into three roughly equivalent bands, each devoted to a different control mode. The range of the upper band varies the shunt from "full on" at its high level to "full off" at its low level. The middle band similarly varies the charge regulator, and the lower band inversely varies the boost from "full off" at its high level to "full on" at its low level. The Sequence Control of the charge



(A)



(B)



(C)

Figure 5.1.1-5. Shunt Candidate

regulator is an override control over the normal charge regulator control functions. If the shunt regulator is operating, i.e., it is draining away excess array power, and the battery is fully charged, the charge regulator would probably only be supplying trickle power depending on the charging method used. Any subsequent Sequence Control override signal would in that case not affect the charge regulator operation.

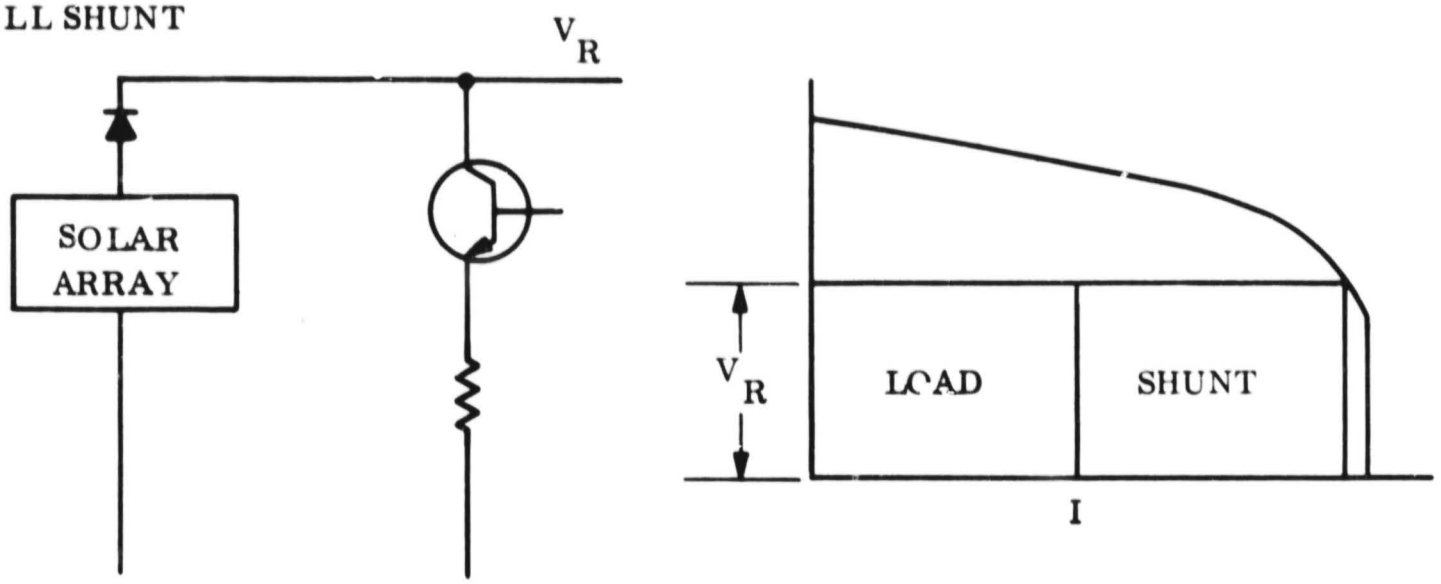
The determination of relative voltage levels is shown on Figure 5.1.1-5c. Again $V_N = 1.25$ provides the maximum power capability at Mars. However, since the array voltage is constant throughout the mission (same as regulated voltage), there would be a power deficiency in near-Earth operation as seen on Figure 5.1.1-1. The selection $V_N = 1.2$ avoids this condition with a penalty of several percent in the power available at Mars.

The 1.5:1 ratio for the relative values of charger input to battery discharge is used as before which results in a similar ratio for the raw power range.

The selection of a partial shunt over a full shunt is based on its lower thermal dissipation within the shunt elements. Figure 5.1.1-6 shows the full and partial shunt options and their modes of operation relative to the solar array V-I curve. If the voltages of the two V-I curves for the partial shunt case were added, they would result in the full shunt V-I curve. As shown on the sketch, these are drawn to scale relative to each other, and it becomes apparent that the partial shunt dissipation is significantly less. It is also clear that the current requirement for both types is about equivalent.

Figure 5.1.1-7 shows the shunt analysis for a solar array quite similar in size to the MM '69 solar panels. This particular array would produce about 900 watts at 1.0 AU at a panel temperature of 100°F. The curve shows the dissipation from either a full or partial shunt for a nominal demand load of 200 watts. The dissipation is shown as a function of array temperature to identify the maximum dissipation that might occur during emergence from an Earth eclipse. Each shunt section has a transistor and resistor in series. The dotted lines indicate the heat dissipation associated only with the transistors which is almost the same for the full and partial shunt cases. It is possible that no resistors will be required for the partial shunt case. It was therefore selected for use in the shunt system candidate.

- FULL SHUNT



- PARTIAL SHUNT - SINGLE SECTION

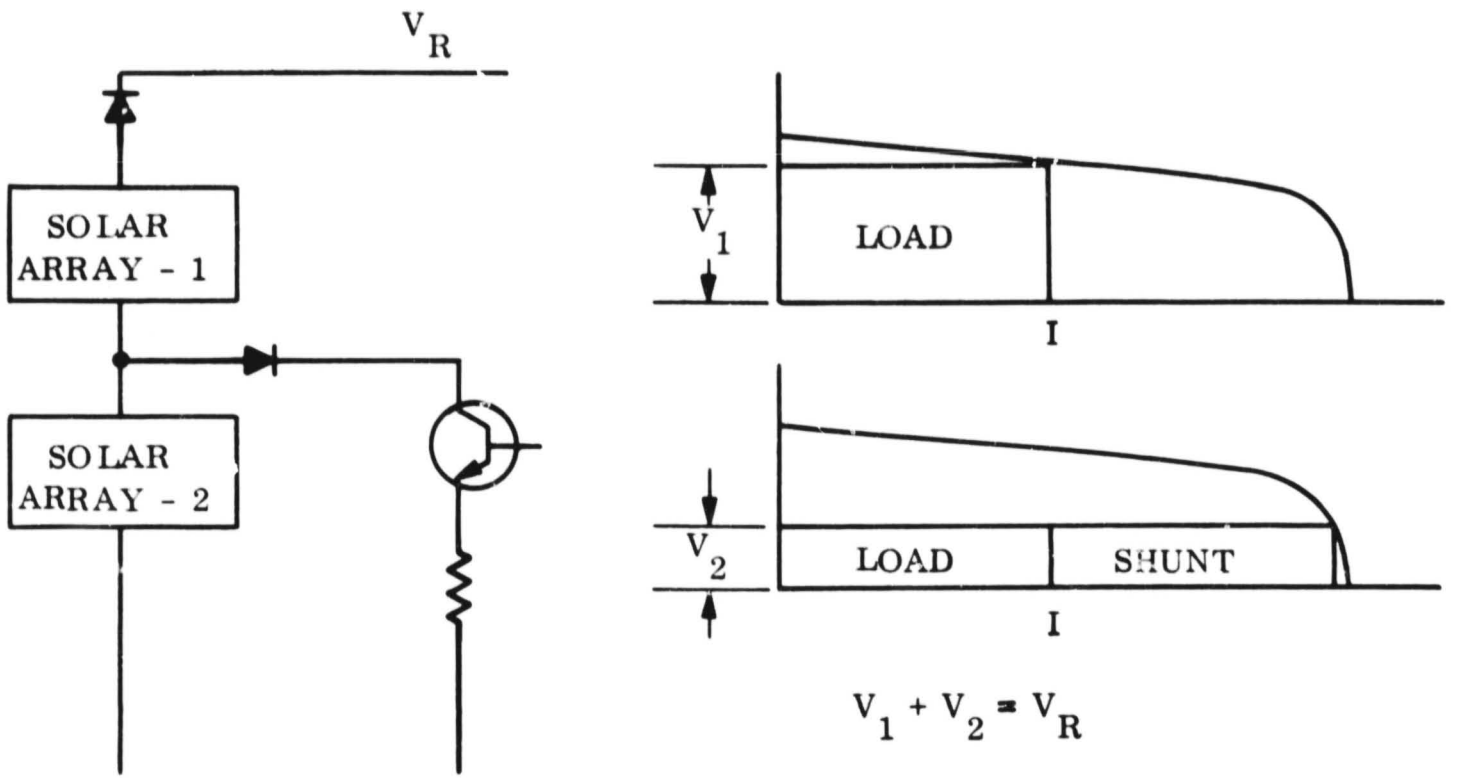


Figure 5.1.1-6. Shunt Regulator Options

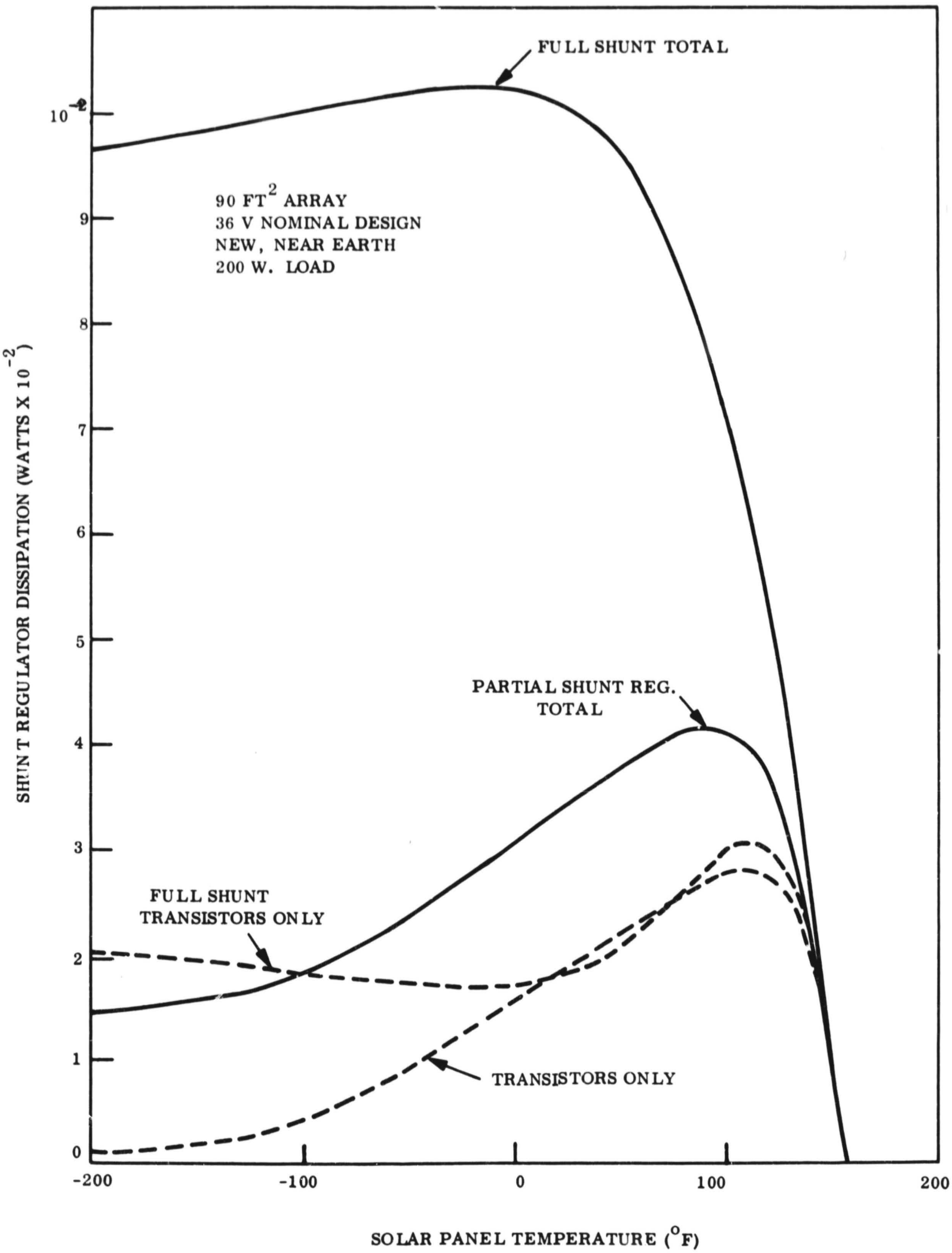


Figure 5.1.1-7. Shunt Performance

5.1.1.4 Candidate Comparison

The three candidate systems are compared on the matrix shown on Table 5.1.1-1. The rating of each candidate against a particular criterion is indicated in the rating columns where "1" indicates the highest rating, "2" the intermediate rating, and "3" the lowest rating. The straight lowest summation of these ratings provides the basis for candidate selection; no attempt was made to weigh the factors.

Pertinent discussion for each criterion is provided below:

Relative Battery Demand

For regulated loads, battery demand in the boost and buck systems is inversely proportional to the regulator efficiency and the discharge diode efficiency, assumed to be 0.97. Then the relative demands are:

$$\frac{\text{Buck demand}}{\text{Boost demand}} = \frac{0.85 \times 0.97}{0.91 \times 0.97} = 0.94$$

using the regulator efficiencies cited in Figure 5.1.1-2. The shunt system does not contain a battery discharge diode to the boost regulator and therefore,

$$\frac{\text{Shunt demand}}{\text{Boost demand}} = \frac{0.85 \times 0.97}{1.00 \times 0.85} = 0.97$$

For raw loads, all three candidates provide battery power to the raw bus through diodes and therefore no battery demand difference exists.

Relative Array Demand

For regulated loads, array demand is inversely proportional to regulator efficiency:

$$\frac{\text{Buck demand}}{\text{Boost demand}} = \frac{0.89}{0.92} = 0.97$$

Table 5.1.1-1. Candidate Comparison

Criterion		Boost	R*	Buck	R*	Shunt	R*
Relative Battery Demand	Reg loads	1.0	3	0.94	1	0.97	2
	Raw loads	1.0	-	1.0	-		-
Relative Array Demand	Reg loads	1.0	3	0.97	2	0.93	1
	Raw loads	1.0	1	1.0	1	1.02	2
	Charge Power	small+	-	small	-	small-	-
Packaging		Compact	2	Compact	1	Shunt wiring	3
Bay Thermal Design		Battery Integr.	-	Battery Integr.	-	Battery Integr.	-
Raw Bus Limits		2:1	2	≥ 1.7:1 (Zeners?)	2	1.5:1	1
Reg Bus Limits		±2%	-	±2%	-	±2%	-
Ripple, day		PWM reg	2	PWM reg	2	Shunt	1
Ripple, night		PWM reg	-	PWM reg	-	PWM reg	-
Response		Medium	-	Medium	-	Medium	-
Battery Charger Integration		Variable Voltage Input	2	Variable Voltage Input	3	Fixed Voltage Input	1
Operational Complexity		Share Boost	2	Share Boost	2	Sequence control, no switching	1
Flexibility/ Growth		Regulator Size Limit	2	Regulator Size Limit	2	Add shunt elements (day operation)	1
Redundancy Implementation		Single Function	1	Single Function	1	Multi-Functions	2

* Rating Scale:
  1 = Highest
  2 = Intermediate
  3 = Lowest

Table 5.1.1-1. Candidate Comparison (cont)

Criterion	Boost	R *	Buck	R *	Shunt	R *
Failure Modes						
Regulator-Array Operation :						
Open	Results in short	2	Complete power loss	2	Minor effect (multiple units)	1
Short	$V_{BUS} < V_{BATT}$	3	$V_{BUS} = V_{ARRAY}$	2	Array section loss	1
Control Failure	$V_{BUS} \geq V_{ARRAY}$	3	$0 \leq V_{BUS} \leq V_{ARRAY}$	2	$V_{BATT} \leq V_{BUS} \leq V_{ARRAY}$	1
Regulator-Battery Operation:						
Open	Results in short	-	Complete power loss	-	Results in short	-
Short	$V_{BUS} < V_{BATT}$	2	$V_{BUS} = V_{BATT}$	1	$V_{BUS} < V_{BATT}$	2
Control Failure	$V_{BUS} \geq V_{BATT}$	1	$0 \leq V_{BUS} \leq V_{BATT}$	2	$V_{BUS} \geq V_{BATT}$	1
Ease of Test On Pad	Wide ground power limits	1	Wide ground power limits	1	Tight ground power limits, shunt simulation probable	2
Flight Demonstration	Yes	1	Partly (Nimbus B)	3	Partly (Lunar Orbiter)	2
TOTALS		33		30		25

* Rating Scale:

1 = Highest
2 = Intermediate
3 = Lowest

$$\frac{\text{Shunt demand}}{\text{Boost demand}} = \frac{0.89}{0.98} = 0.91$$

The shunt system incurs an Earth/Mars matching penalty of several percent and therefore, the relative shunt demand is raised to 0.93.

For raw loads, array power is supplied directly to the raw bus for all candidates. Again the shunt system is penalized by two percent to raise its relative demand to 1.02.

For charge power, small differences in charge power are associated with the relative battery demand--this is not significant as a measure.

Packaging

No major differences are involved. The bay equipment is about the same for all candidates. The buck system may or may not require zener shunts on the array. The boost system requires zeners; the shunt system requires transistors plus additional wiring for the base drives. Therefore, they are rated 1, 2, 3 in that order.

Bay Thermal Design

No significant difference. Main thermal problem is probably battery integration which is common to all candidates.

Raw Bus Limits

Limits are indicated on Figures 5.1.1-3, 5.1.1-4 and 5.1.1-5.

Regulated Bus Limits

No measure--similar limits should be achievable with pulse width modulated electronics of all candidates.

Ripple, day; with array power, the shunt system should be best since switching electronics are not in use.

Ripple, night; no measure--with battery power, switching electronics are used in all candidates.

Response; no measure--all candidates depend on response of switching electronics.

Battery Charger Integration

A smaller variation in the charger input voltage results in a smaller average drop through the regulator resulting in more efficient power usage. The shunt system, with a fixed charger input voltage, is best in this regard. The buck system may or may not be worse than the boost system depending on whether or not zener array voltage limiters are used.

Operational Complexity

The boost and buck systems require some means for avoiding solar array/battery load sharing while the shunt system requires a sequence control. Since no switching of relays are required for the shunt system, it is rated better.

Flexibility/Growth

Power capability during array operation for the boost and buck system is limited by the regulator ratings. The growth of the shunt system is accommodated by adding shunt elements. (Shunt control can be initially designed for possible growth.) During battery operation all systems are limited by regulator size.

Redundancy Implementation

Redundancy schemes for the shunt system may be complicated by multifunctions operating from a single Sequence Control.

Failure Modes

Regulator-Array Operation

a. Open power transistor: Circuit review of the boost regulator indicates that an open circuit of one transistor would result in a short to ground of the remaining transistor with complete power loss; the bypass diode capability would be ineffective. An open transistor in the buck regulator obviously results in complete power loss. An open

shunt transistor of the shunt system results in no power loss; the system can be easily designed to permit several such failures with remaining transistors absorbing the additional shunt load.

b. Shorted power transistor: For the boost regulator circuit, this is a short to ground with probable full power loss. For the buck regulator, this is a through short and the output is the same as the array voltage input. A shorted shunt transistor only results in loss of the associated array section.

c. Control failure: With bypass diode capability in the boost regulator the output could be higher but no less than the array input voltage. Inherently the buck regulator cannot produce an output voltage higher than its input; therefore, a control failure could result in output between zero and the highest array input. With the shunt system the array voltage and bus voltage are identical; this voltage can be drawn downward to the battery voltage by virtue of the bypass diode capability of the battery discharge boost regulator.

Regulator-Battery Operation

a. Open power transistor: Complete power loss for all candidate systems--no measure.

b. Shorted power transistor: Probable complete power loss for boost system or shunt system due to short to ground of boost regulator. Through short of buck regulator results in bus voltage same as battery voltage.

c. Control failure: With bypass diode capability in boost regulator the output could be higher but no less than the battery input voltage; this applies to the boost and shunt systems. Buck regulator maximum output is limited to battery input voltage.

Ease of Test-On Pad

Both the boost and buck systems can accept wide variations in ground power voltage during on-pad operations by way of array simulation or other power supplies. The boost and buck regulators automatically condition this raw input. The shunt system cannot function in this way since the shunt transistors are diode isolated on the solar array. Until appropriate solutions are found, the shunt system is rated lower on this criterion.

Flight Demonstration

The boost system has been used extensively on Mariner and Ranger spacecraft. The buck system has been used on battery powered military satellites and is used on the Nimbus B

spacecraft. The shunt system was used on the Lunar Orbiter spacecraft in a somewhat different arrangement.

The summation of ratings resulted in the selection of the shunt system as the candidate for further comparison with the MM '69 power system.

5.1.2 DISTRIBUTION FREQUENCY OPTIMIZATION

Much of the power of the MM '69 spacecraft is ac distributed at a frequency of 2.4 kHz. This section provides an analysis of whether this frequency is near optimum from the standpoint of weight. The only constraint is that the wave form be essentially square.

The principal elements whose weights are affected by frequency are: (a) dc/ac inverters; (b) ac/dc transformer-rectifiers; (c) power source equipment whose size is affected by possible efficiency changes in the inverters and transformer-rectifiers. Each of these elements are considered separately below.

5.1.2.1 Inverter Weight

As a function of frequency, inverter weight is primarily sensitive to power transformer weight. The weight of the power switch transistors and drive circuits in comparison to the output power transformer is relatively constant. Thus transformer weight as a function of frequency may be studied separately since the results will provide the most sensitive data for observing inverter weight effects.

5.1.2.1.1 Transformer Weight

Transformer size depends on power output, efficiency, temperature rise, voltage levels, and frequency. Specific designs were analyzed and the results are plotted in Figure 5.1.2-1. The frequency was varied from 60 to 5000 Hz under the following constraints:

a. Power level is constant.

b. Efficiency is constant--hence for equal assembly materials and procedures temperature rise is also considered constant.

c. Voltage levels are not in a range where extra insulation affects size or weight.

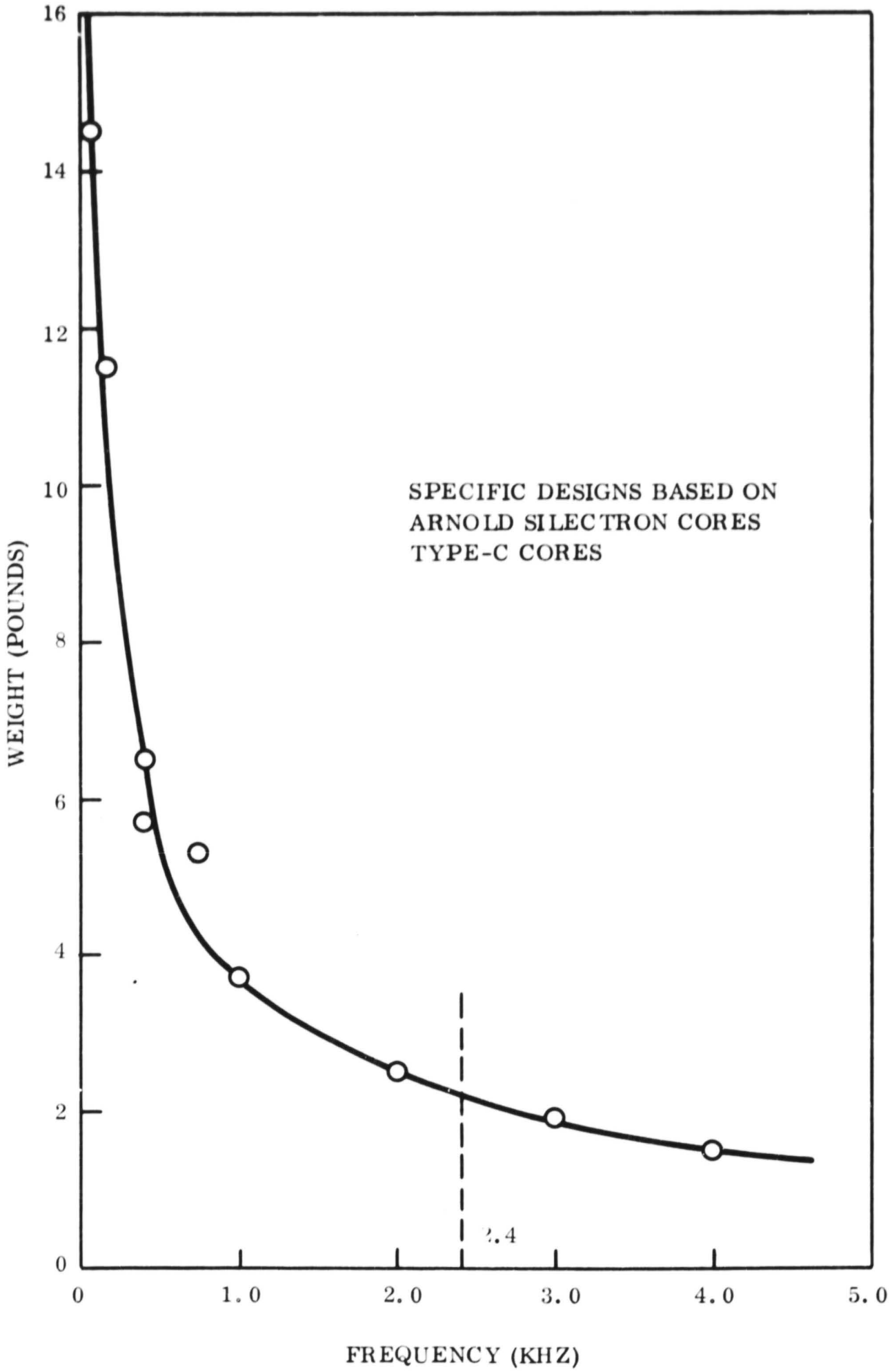


Figure 5.1.2-1. Transformer Weight-200 Watt Output, 97 Percent Efficiency

In addition to the designs of Figure 5.1.2-1, a search was conducted to obtain results of other design procedures. The results of this search and Figure 5.1.2-1 are plotted in Figure 5.1.2-2 with reference to 60 Hz transformer size. The levels in this figure are relative and are representative of three design procedures as a function of frequency. Note that regardless of procedure, the percent change in weight beyond 1000 to 2000 Hz is not appreciable as frequency is increased. *+

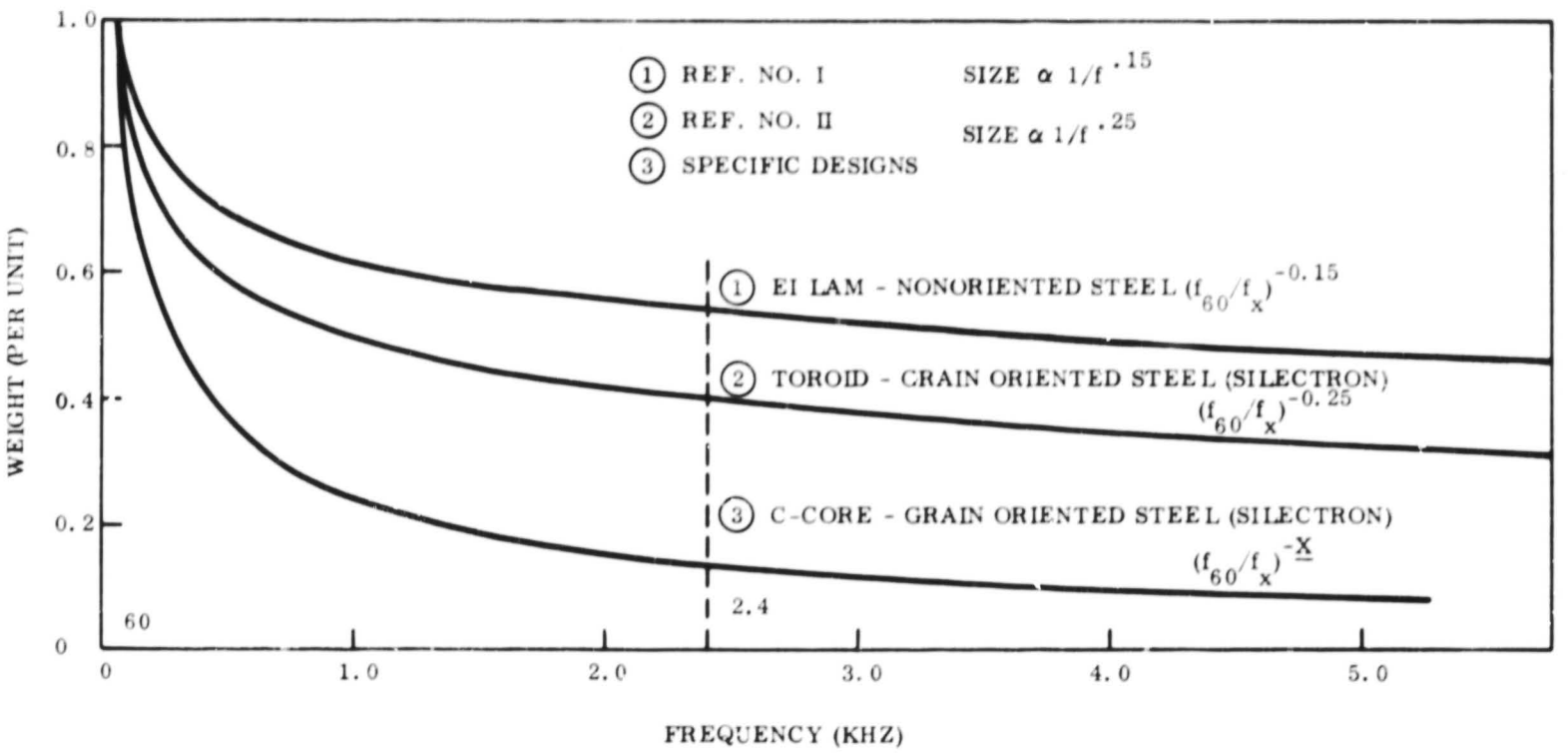


Figure 5.1.2-2. Transformer Weight Percent Reference to 60 Hz

5.1.2.1.2 Transformer-Rectifier (T/R) Weight

The same assumptions established for determining inverter weight sensitivity to frequency are directly applicable to the T/R weight The curve generated for the inverter/transformer weight is directly applicable to T/R weight.

---

* Ref. No. I, "Voltage Regulation and Conversion in Unconventional Electrical Generator Systems", Bureau of Weapons, Dept. of Navy, Contract No. NOw62-0984d. Section 5.4, pp 108.

+ Ref. No. II, "Transformers for Electronic Circuits", Nathan R. Grossner, pp. 109.

5.1.2.1.3 Preliminary Conclusion

Based on the weight of the inverters and T/R's, a preliminary conclusion is that operation beyond 1.5 kHz does not provide sufficient weight gain to merit its consideration. To substantiate this conclusion, the question of overall power system weight effects must be answered. The parameter which affects solar array and battery sizing is inverter and T/R efficiency. This parameter is examined in the following sections.

5.1.2.2 Inverter Efficiency

Inverter efficiency is mostly affected by transistor and transformer losses. The transformer losses are relatively constant over a wide range of frequency. The transistor and diode losses, on the other hand, are sensitive to frequency and are accordingly treated below.

5.1.2.2.1 Transistor Efficiency

The power switch operates either full on or full off with a finite time required for transfer. This transfer time is determined by intrinsic transistor characteristics and results in switching power losses. The more frequent the switch transfers the greater are the switching losses.

Since power transformer efficiency is constant by design, the inverter efficiency can be analyzed by considering only power switching losses as a function of frequency. These losses are expressed by the following equation which is derived in Section 5.1.2.4.

$$P_{sw} = fV_{in} I_c \left[0.71\, t_s + 4/3 \left(\frac{t_s\, t_f}{t_s + t_f} \right) + 5/3 \left(\frac{t_f^2}{t_s + t_f} \right) + 0.33\, t_f \right] X$$

$$\left[\frac{1}{1 - 4f\,(t_s + t_f)} \right]$$

where:

P_{sw}	is power switch loss in watts (P_{sw} occurs twice per cycle)
f	is frequency
V_{in}	is supply voltage less $V_{ce_{SAT}}$
I_c	is peak collector current
t_s	is storage time
t_f	is fall time

5.1.2.2.2 Rectifier Efficiency

Rectifier efficiency is treated similarly to the transistor switch efficiency as a function of frequency. The losses are expressed by the following equation, which is derived in Section 5.1.2.4.

$$P_{rsw} = fV_R I_D 1/6\, t_{rec}$$

where

P_{rsw}	is power rectifier switching loss in watts
f	is frequency
V_R	is peak reverse voltage seen by rectifier
I_D	is rectifier peak current
t	is recovery time of diode

P_{rsw} occurs twice per cycle.

Since recover time of diodes is at least an order of magnitude faster than transistor switching times, it is considered negligible in this analysis for the frequency range considered.

5.1.2.2.3 Inverter Efficiency Results

Transistor switching losses along with other transistor losses (drive losses and saturation losses) were used in a computer program to determine inverter efficiency as a function of frequency. The results are shown in Figure 5.1.2-3 for an inverter of the Mariner '69

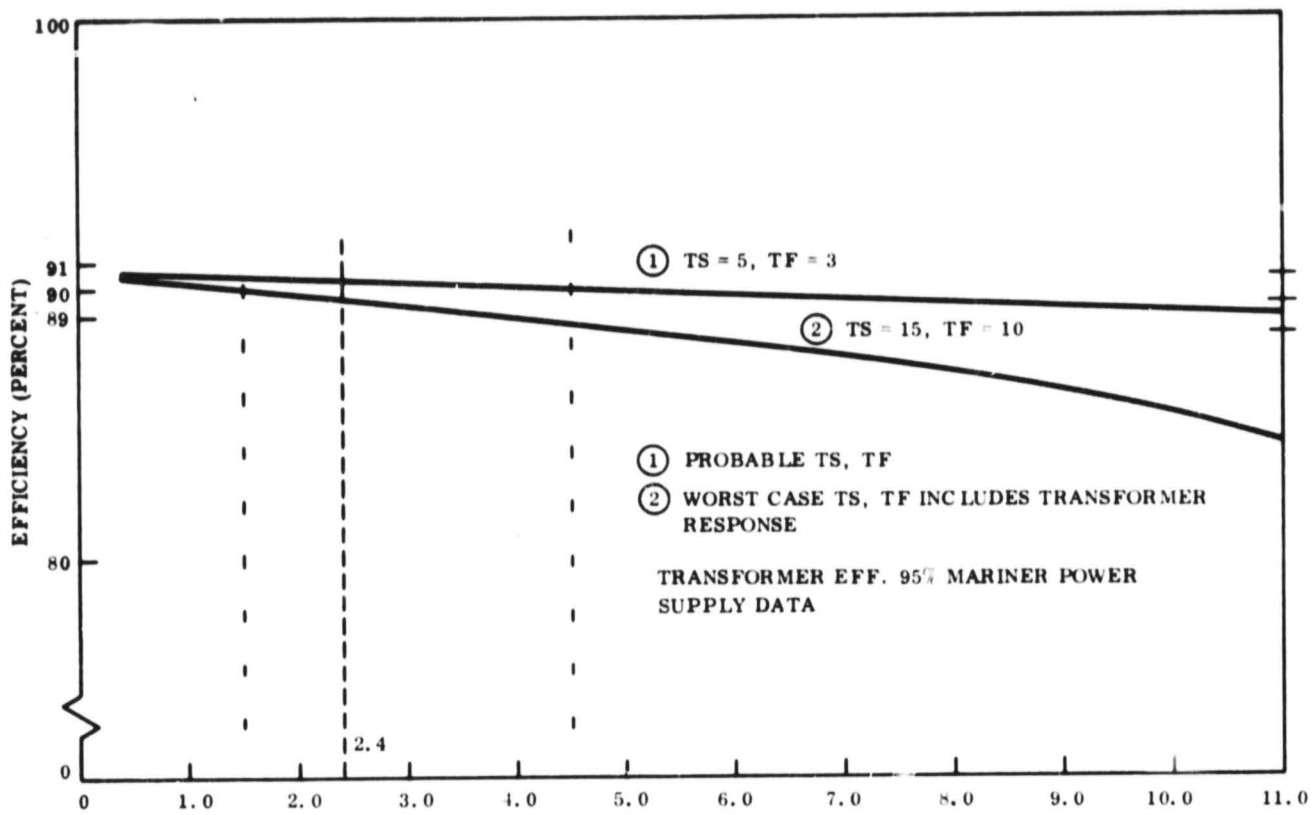


Figure 5.1.2-3. Square Wave Inverter Efficiency

design for two sets of t_s and t_f. This range is considered the range of best to worst cases for present transistors and circuit configurations.

5.1.2.3 Power Source Weight

Based on a Mariner load profile, the specific weight in pounds per watt at the inverter input can be determined when the inverter operates from the solar array only and from the battery only. Table 5.1.2-1 derives the specific weight (0.288 lb/watt) for the solar array, and Table 5.1.2-2 derives the specific weight (0.117 lb/watt) for the battery.

Using these specific weights and knowing the inverter efficiency and transformer weight as a function of frequency, total power system weight can be determined as a function of frequency. The results are tabulated in Table 5.1.2-3 for several values of frequency and the bracketing values of t_s and t_f.

Table 5.1.2-1. Primary Power Source Weight - Pounds per Watt at Inverter Input

- Orbiter load profile
- Far Encounter phase - Solar Array Case
- 2.4 kHz Inverter load = 214 w
- Inverter Input (214/0.918) = 233 w
- Inverter load reflected at array

  Boost Reg. Efficiency = 0.887
  Distribution Losses = 0.97

  $$\frac{214}{0.918 \times 0.887 \times 0.97} = 271 \text{ w}$$

- Total array demand = 421 w
- Percent array for inverter loads = $\frac{271}{421} = 64\%$
- Array Weight:

  Cell ass'y - 50 lb
  Structure - 54.5 lb
  104.5

- Percent array weight for inverter loads 0.64 x 104.5 = 67 lb
- Array weight per watt at inverter input =

  $$\frac{67}{233} = 0.288 \text{ lb/watt}$$

Table 5.1.2-2. Secondary Battery Source Weight - Pounds per Watt at Inverter Input

- Orbiter load profile
- Orbit insertion phase - Battery Case
- 2.4 kHz Inverter load = 179.5 w
- Inverter input (179.5/0.910) = 197 w
- Inverter load reflected at battery

  Boost Regulator efficiency = 0.842
  Distribution loss = 0.97

  $$\frac{179.5}{0.910 \times 0.842 \times 0.97} = 242 \text{ w}$$

- Total Battery demand = 326 w
- Percent battery for inverter = $\frac{242}{326} = 74\%$
- Battery weight = 31 lb
- Percent battery weight for inverter = 0.74 x 31 = 23 lb
- Battery weight per watt at inverter input = $\frac{23}{197} = 0.117$ lbs/watt

Table 5.1.2-3. Power System We'ght

FREQ Hz	Inverter Load SA/B	Inverter Efficiency	Inverter Input SA/B	Total Transformer Weight	Solar Array Weight	Battery Weight	Total Weight
$t_s = 5$, $t_f = 3$							
1,000	214/180	0.905	236/198.9	7.4	68.0	23.2	98.6
2,400	214/180	0.904	237/199.2	4.4	68.3	23.3	96.0
4,000	214/180	0.900	238/200	3.0	68.6	24.0	
$t_s = 15$, $t_s = 10$							
1,000	214/180	0.902	237.5/199.5	7.4	68.4	23.3	99.1
2,400	214/180	0.896	239/201	4.4	68.8	23.5	96.7
4,000	214/180	0.888	241/203	3.0	69.4	23.7	96.1
6,000	214/180	0.879	244/205	2.6	70.2	24.0	96.8

Total Trans Wt. Includes T/R and Inverter.

Weight - pounds
Array - 0.288 lb/watt
Battery - 0.117 lb/watt
SA/B - Solar Array/Battery

5.1.2.3.1 Conclusions

The results of Table 5.1.2-3 indicate that frequency has little effect on weight within the frequency range examined. While operation at 4 kHz appears optimum, the weight gain is only about 0.5 pounds (or 0.5 percent) compared to that at 2.4 kHz. This provides little incentive for considering a change from the frequency presently used on the MM '69 system. These results are consistent for the extremes of t_s and t_f considered.

5.1.2.4 Inverter Efficiency Analysis

This analysis considers the effect of operation frequency on inverter efficiency. The inverter efficiency is mostly affected by transistor losses and transformer losses. In addition, the affects of load transformer-rectifier (T/R) must also be considered. Transformer losses are, by design, relatively constant over a wide frequency range. The transistor and rectifier losses on the other hand are sensitive to frequency and are accordingly treated below.

5.1.2.4.1 Transistor Switching Losses

The switching losses are determined by intrinsic switch characteristics. These characteristics are altered by drive control and load. Drive control is primarily determined by load current magnitude, and it affects switching losses only if insufficient reverse bias is provided during the switch off time. Assuming that drive control conditions are adequate, load is the only remaining parameter to affect the intrinsic characteristics of the transistor switch. Part of the real load is the power transformer, and it is examined along with load to establish the conditions during switch transfer from on to off.

The equivalent circuit seen by the transistor switch is shown in Figure 5.1.2-4. Switches Q1 and Q2 are the power transistors, T is the ideal transformer, R_L is the nominal load, and the balance is the transformer impedances seen by the power switch. The transformer impedances somewhat distort the desired square wave. Further, the switches are not considered fully open or closed until the transformer is in a stable state. Thus, the transistor switching time is affected by the transformer frequency response. Note that high frequency characteristics are desirable for the transformer.

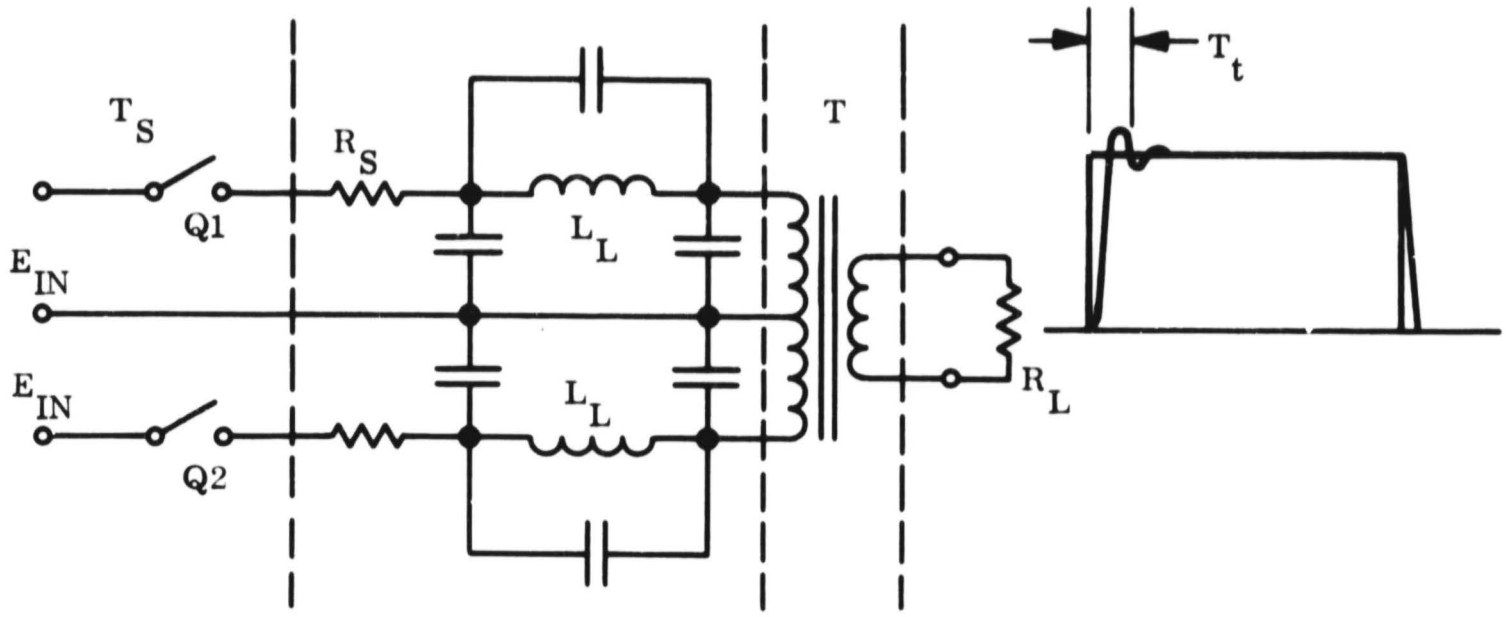


Figure 5.1.2-4. Transformer Equivalent Circuit

The design of transformers with high frequency response involves many factors. Their effect may be analyzed indirectly by considering switching losses over a wider range than those suggested by the transistor manufacturer.

5.1.2.4.2 Transistor Switching Diagrams

The transistor switching diagram for a push-pull configuration is shown in Figure 5.1.2-5. The switch forcing function is the drive power shown in time only for Q1 and Q2. Consider that Q1 is on and the level of collector current I_c is determined by R_L. At time t_1 the drive to Q1 is removed and drive to Q2 is applied. Collector current of Q1 continues to flow due to load effects and transistor storage time, t_s. Transistor Q2 starts to turn on denoted by the fall of V_{ce} and rise of I_{c2}. Since Q1 is still on and Q2 is turning on, the high impedance normally presented by the transformer is reduced such that I_c of Q2 rises to a level determined by transistor drive current and gain. For this analysis a gain limit of two times that required is assumed. Therefore, I_{c2} rises to $2I_{c2}$ until Q1 begins to open such that the

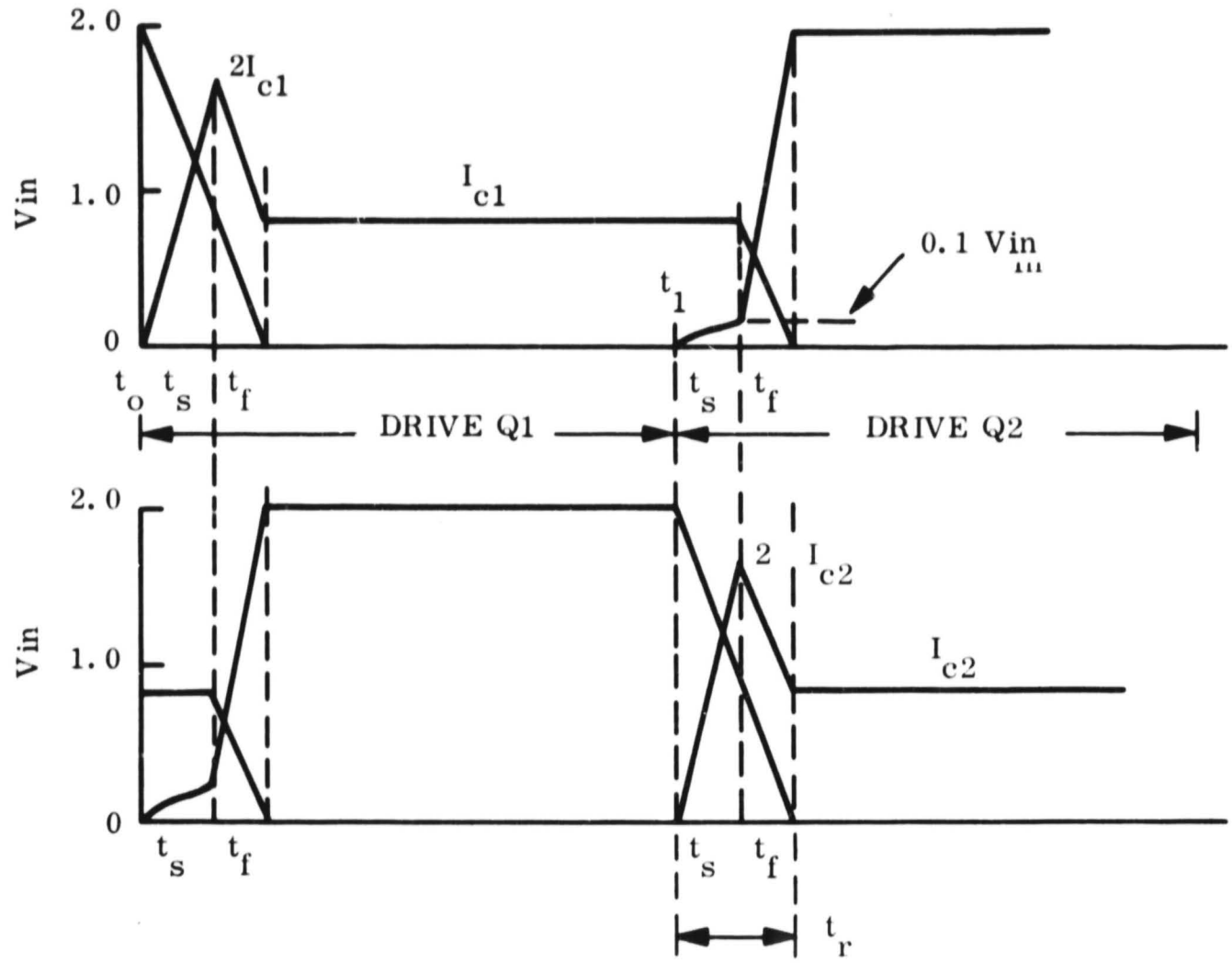


Figure 5.1.2-5. Switch Voltage-Current-Time Diagram of Push-Pull Inverter

impedance presented by the transformer increases reducing I_{c2} to I_{c2} level determined by R_L. Thus, the diagram shows the relation between rise, fall, and storage time of a transistor. Note that the rise time, t_r, is a function of t_s and t_f. The switching diagram associated with the time diagram is Figure 5.1.2-6. The power dissipated during the switching period is then the summation of each period of t_r, t_s, t_f; where t_r is f (t_s, t_f).

5.1.2.4.3 Power Dissipation General Case

Since the voltage-current for each time period of the diagram can be considered linear, a general case power dissipation for each time period may be derived. Consider the general case for linear switching shown in Figure 5.1.2-7. The instantaneous current is

$$i = I_x + \left(\frac{I_y - I_x}{t_1} \right) t,$$

and the instantaneous voltage is

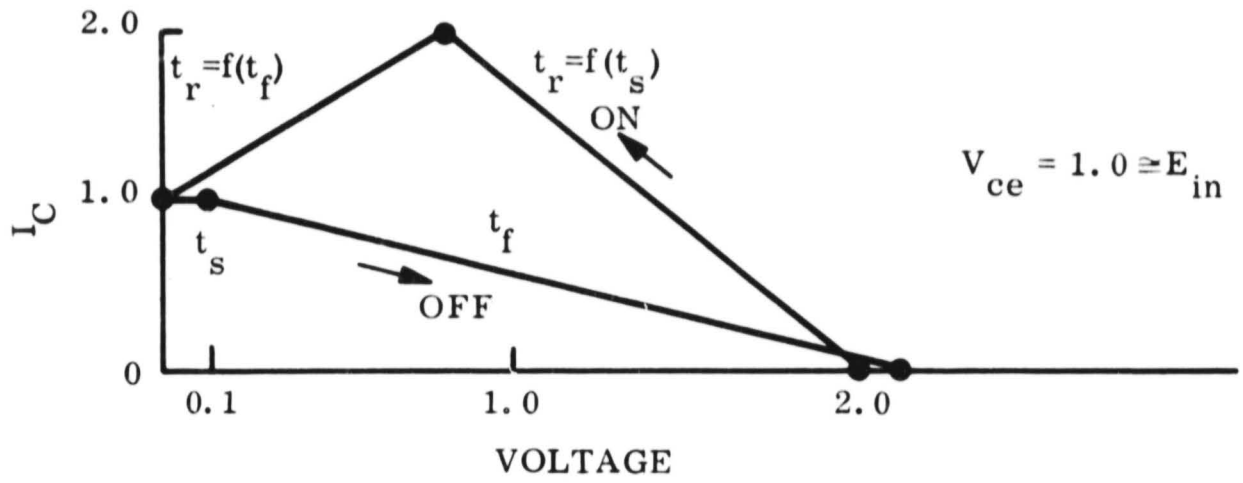
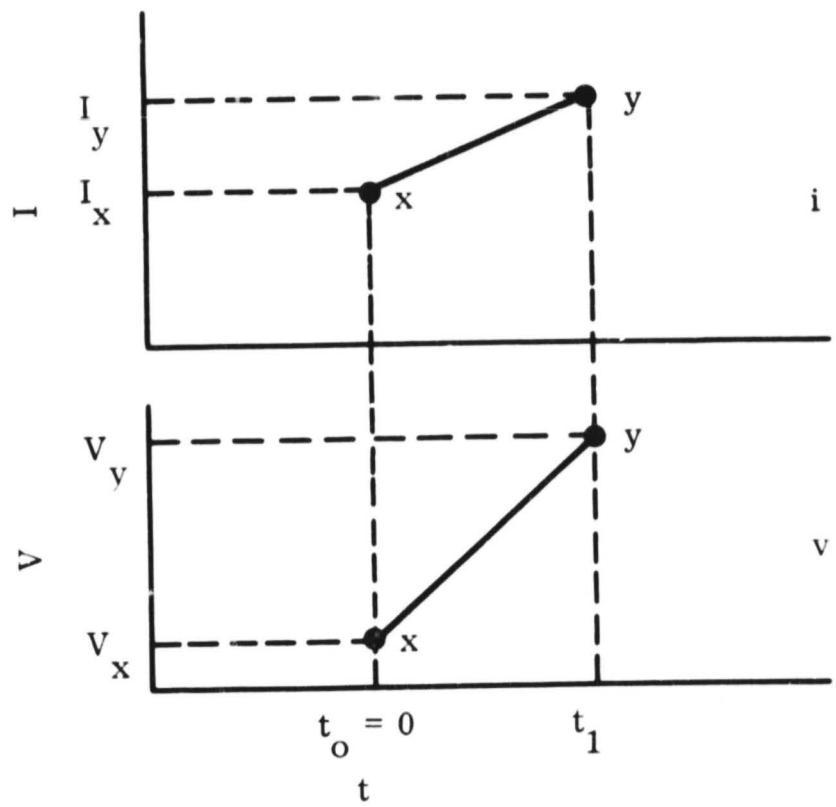


Figure 5.1.2-6. Switching Diagram



$$i = I_x + \left(\frac{I_y - I_x}{t_1} \right) t$$

$$v = V_x + \left(\frac{V_y - V_x}{t_1} \right) t$$

Figure 5.1.2-7. Linear Switching

$$v = V_x + \left(\frac{V_y - V_x}{t_1} \right) t.$$

The power for this interval is

$$P = \frac{1}{T} \int_0^{t_1} v\, i\, dt,$$

where T is the period of **reoccurrence.**

This equation reduces to

$$P = \frac{1}{T}\, t_1 \left[1/6\, (V_x I_y + V_y I_x) + 1/3\, (V_y I_y + V_x I_x)\right].$$

Thus each interval is examined using this equation and the total switching losses is a summation of each interval during period T where T is $\frac{1}{f}$ and f is frequency of operation.

5.1.2.4.4 Derivation of Transistor Switch Loss

The general equation for linear switching is

$$P = ft \left[1/6 (V_x I_y + V_y I_x) + 1/3\, (V_y I_y + V_x I_x)\right].$$

Referring to Figure 5.12-5, at Q2 turnon the rise time, t_r, is shown in two parts. The first is shown related to storage time, t_s, and the second is shown related to fall time, t_f. Power loss during this time period is

$$P_r = f(t_s) + f(t_f) \equiv P_r (t_s + t_f).$$

Since V_{ce} nearly equals $2V_{in}$ when the transistor is off, V_{in} is used for clarity because V_{ce} appears later when the transistor is on. For the switching period calculations the transistor $V_{ce_{SAT}}$ is considered zero since the error is much less than one percent.

The power loss during rise time is as follows:

P_r (Part 1)

$$P_r(t_s) = f\,t_s\left[1/6\,(2V_{in}\;2I_c + 0) + 1/3\,(2V_{in}\;\frac{t_f}{t_s + t_f}\;2I_c + 0)\right]$$

$$P_r(t_s) = f\,V_{in}\,I_c\,(2/3\,t_s + 4/3 \cdot \frac{t_s\,t_f}{t_s + t_f})$$

P_r (Part 2)

$$P_r(t_f) = f\,t_f\left[1/6\,(2V_{in}\;\frac{t_f}{t_s + t_f}\;I_c + 0) + 1/3\,(0 + 2V_{in}\;\frac{t_f}{t_s + t_f}\;2I_c)\right]$$

$$= f\,V_{in}\,I_c\,(1/3\;\frac{t_f^2}{t_s + t_f} + 4/3\;\frac{t_f^2}{t_s + t_f})$$

$$P_r(t_f) = f\,V_{in}\,I_c\,(2/3\,t_s + 4/3\;\frac{t_s\,t_f}{t_s + t_f} + 5/3\;\frac{t_f^2}{t_s + t_f})\,.$$

Power loss during the storage time is $P_s(t_s)$.

$$P_s = f\,t_s\left[1/6\,(0 + 0.1\,V_{in}\,I_c) + 1/3\,(0.1\,V_{in}\,I_c + 0)\right]$$

$$P_s = f\,V_{in}\,I_c\,(0.05\,t_s)$$

Power loss during the fall time is $P_f\ (t_f)$.

$$P_f = f\ t_f \left[1/6\ (0 + 2V_{in}\ I_c) + 1/3\ (0 + 0.1\ V_{in}\ I_c \rightarrow 0)\right]$$

$$P_f = f\ V_{in}\ I_c\ (1/3\ t_f)\ .$$

The total switch losses are

$$P_{sw}\ \text{loss} = P_r + P_s + P_f \equiv$$

$$P_{sw}\ \text{loss} = f\ V_{in}\ I_c \left[0.71\ t_s + 4/3\ \frac{t_s\ t_f}{t_s + t_f} + 5/3\ \frac{t_f^2}{t_s + t_f} + 1/3\ t_f\right] \qquad \text{(Eq-1)}$$

This power loss due to switching is described by f, V_{in}, I_c, t_s, t_f. (Note that this loss occurs twice per cycle.)

Note that if frequency increases, the percent time that the transistor is on becomes less. Therefore, in order to supply the same average load current the peak collector current I_c must increase as frequency increases. The derived factor (from next paragraph) for this is,

$$\left[\frac{1}{1 - 4f\ (t_s + t_f)}\right] \qquad \text{(Eq-2)}$$

5.1.2.4.5 Collector Current Frequency Correction

In terms of transistor efficiency as a function of frequency where the average current is a constant and the percent of on time decreases due to fixed switch time and shorter on time, I_c increases as a function of frequency to maintain the average current.

$$I_{AVE} = K_A \equiv \text{Constant per load requirements}$$

$$I_{AVE} = I_c \text{ at frequency equal to zero}$$

then $I_{AVE} = K_f I_c$ at frequency greater than zero, where K_f is a factor which changes as a function of frequency causing I_c also to change in order to maintain a constant I_{AVE}. The factor K_f is determined by reference to Figure 5.1.2-8 and the following text.

For simplicity it is assumed that no power is delivered to the load during the periods $(t_s + t_f)$. Then

$$I_{AVE} = \frac{\frac{1}{2f} - 2(t_s + t_f)}{\frac{1}{2f}} \; I_c$$

where:

$$\frac{\frac{1}{2f} - 2(t_s + t_f)}{\frac{1}{2f}} \equiv K_f .$$

K_f simplified is $1 - 4f(t_s + t_f)$

If K_f decreases as a function of frequency I_c must increase as a function of frequency by the inverse of K_f in order to maintain a constant I_{AVE}. Thus, I_c is corrected for frequency by

$$\left[\frac{1}{1 - 4f(t_s + t_f)} \right] .$$

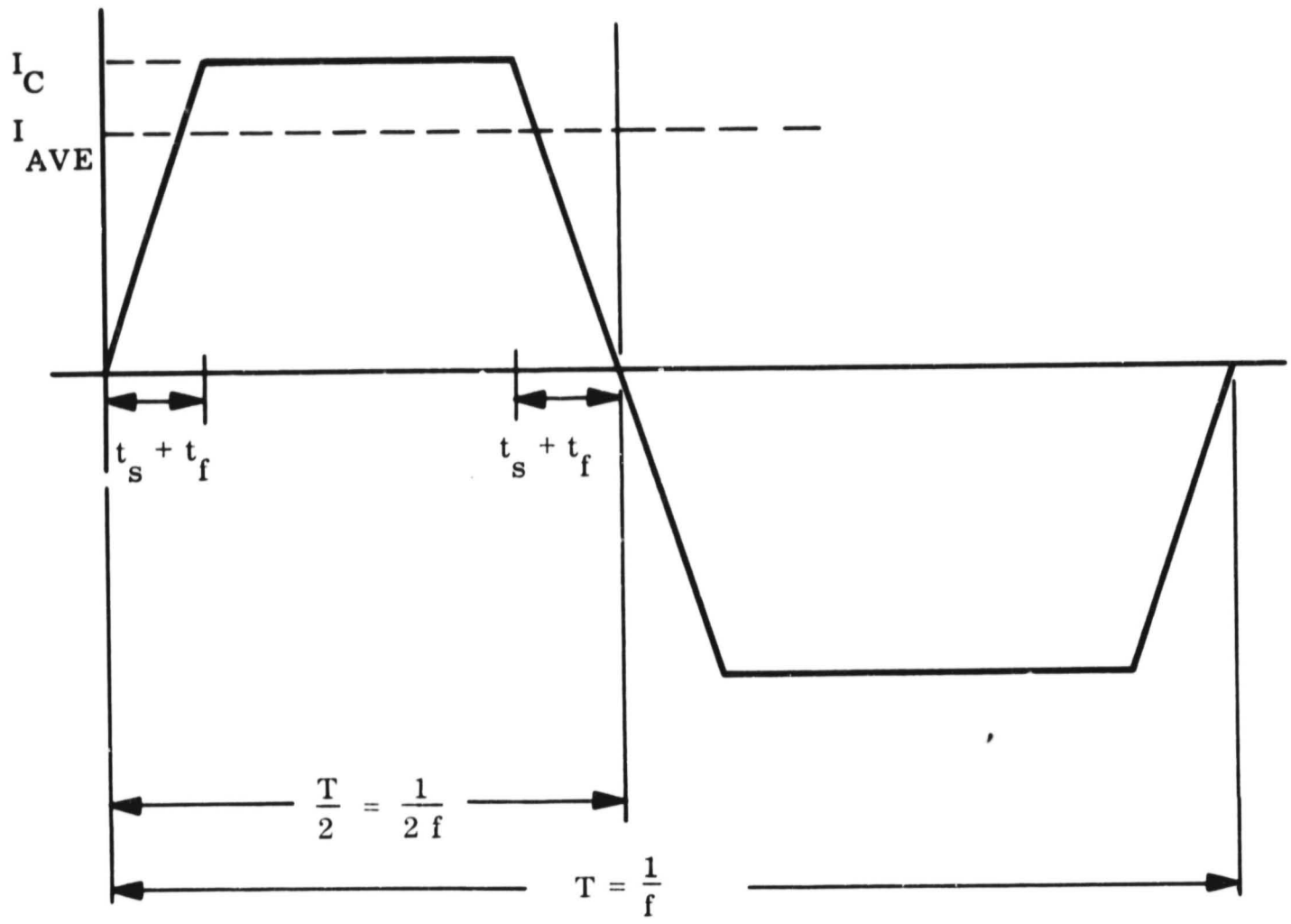


Figure 5.1.2-8. Inverter Collector Current-Time Diagram

Note that if the peak I_c increases then the base drive must correspondingly increase, therefore the base drive must also be adjusted by the same factor. Note also that saturation losses increase by the same factor and is accordingly adjusted.

The inverter efficiency is

$$\eta = \frac{\text{P output}}{\text{P output + Transformer loss + Transistor loss}} ,$$

$$\eta = \frac{P_o}{P_o + (0.05)\, P_o + \text{Transistor loss}} \text{ , with a 95 percent efficient transformer}$$

$$\eta = \frac{1}{1.05 + \frac{\text{transistor loss}}{P_o}} .$$

Knowing transistor losses permits calculation of efficiency.

Transistor losses are

$$P_{total} = 2P_{sw} + P_{drive} + P_{sat}$$

where:

P_{sw} = EQ 1,

P_{drive} = 0.025 P_o, and

P_{sat} = $V_{ce_{SAT}} I_c$ where P_{sw}, P_{drive}, P_{SAT} are corrected by multiplying by EQ 2 since all are related to I_c.

A computer program was prepared where t_s, t_f, V_{ce}, I_c, $V_{ce_{SAT}}$, P_o are inputs, f is varied from 400 Hz to 11,000 Hz, and outputs are P_{sw}, P_{drive}, P_{SAT}, P_{total}, EFF (η). A computer printout for two cases are in Table 5.1.2-4.

Table 5.1.2-4. Computer Printout for Inverter Efficiency as a Function of Frequency

```
READY
$FORT

          CALCULATION OF TRANSISTOR SWITCHING LOSSES

 TS   TF   VIN   IC   VCE   PL= 5   3   55.3   4   .7   200

      F         PSW      PSAT    PDRIVE   PTOTAL       EFF

   400.0     0.079    2.804    7.409    10.371     0.908
  1000.0     0.198    2.809    7.424    10.628     0.907
  1500.0     0.297    2.814    7.436    10.844     0.906
  2000.0     0.397    2.818    7.448    11.060     0.905
  2500.0     0.497    2.823    7.460    11.276     0.904
  3000.0     0.597    2.827    7.472    11.494     0.903
  3500.0     0.698    2.832    7.484    11.712     0.902
  4000.0     0.799    2.836    7.496    11.930     0.901
  5000.0     1.002    2.846    7.520    12.370     0.899
  7000.0     1.412    2.864    7.570    13.258     0.896
  9000.0     1.827    2.883    7.619    14.157     0.892
 11000.0     2.248    2.902    7.670    15.069     0.889


 TS   TF   VIN   IC   VCE   PL= 15   10   55.3   4   .7   200

      F         PSW      PSAT    PDRIVE   PTOTAL       EFF

   400.0     0.254    2.811    7.430    10.749     0.906
  1000.0     0.639    2.828    7.475    11.582     0.903
  1500.0     0.964    2.843    7.513    12.283     0.900
  2000.0     1.292    2.857    7.551    12.992     0.897
  2500.0     1.623    2.872    7.590    13.708     0.894
  3000.0     1.958    2.887    7.629    14.431     0.891
  3500.0     2.296    2.902    7.668    15.162     0.888
  4000.0     2.638    2.917    7.708    15.900     0.885
  5000.0     3.332    2.947    7.789    17.400     0.880
  7000.0     4.765    3.011    7.957    20.497     0.868
  9000.0     6.260    3.077    8.132    23.730     0.856
 11000.0     7.824    3.146    8.315    27.108     0.843
```

5.1.2.4.6 Rectifier Switching Losses

Using the general equation for linear switching derived previously, the diode rise and fall time losses are derived with reference to Figure 5.1.2-9 as follows:

The rectifier voltage-current curve shows that very little power is lost in the diode during the rise time. The primary power loss is during the fall time, which is the diode recovery time.

$$P = ft\,[1/6\,(V_x I_y + V_y I_x) + 1/3(V_y I_y + V_x I_x)]$$

$$P_f = ft\,[1/6\,(0 + V_R I_D) + 1/3\,(0 + 0)]$$

$$P_f = fV_R I_D\, 1/6\, t_{rec}, \qquad \text{(Eq 3)}$$

where:

P_f is power rectifier switching loss in watts.

t is time

f is frequency

V_R is reverse voltage seen by rectifier

I_D is forward current at time of switching off

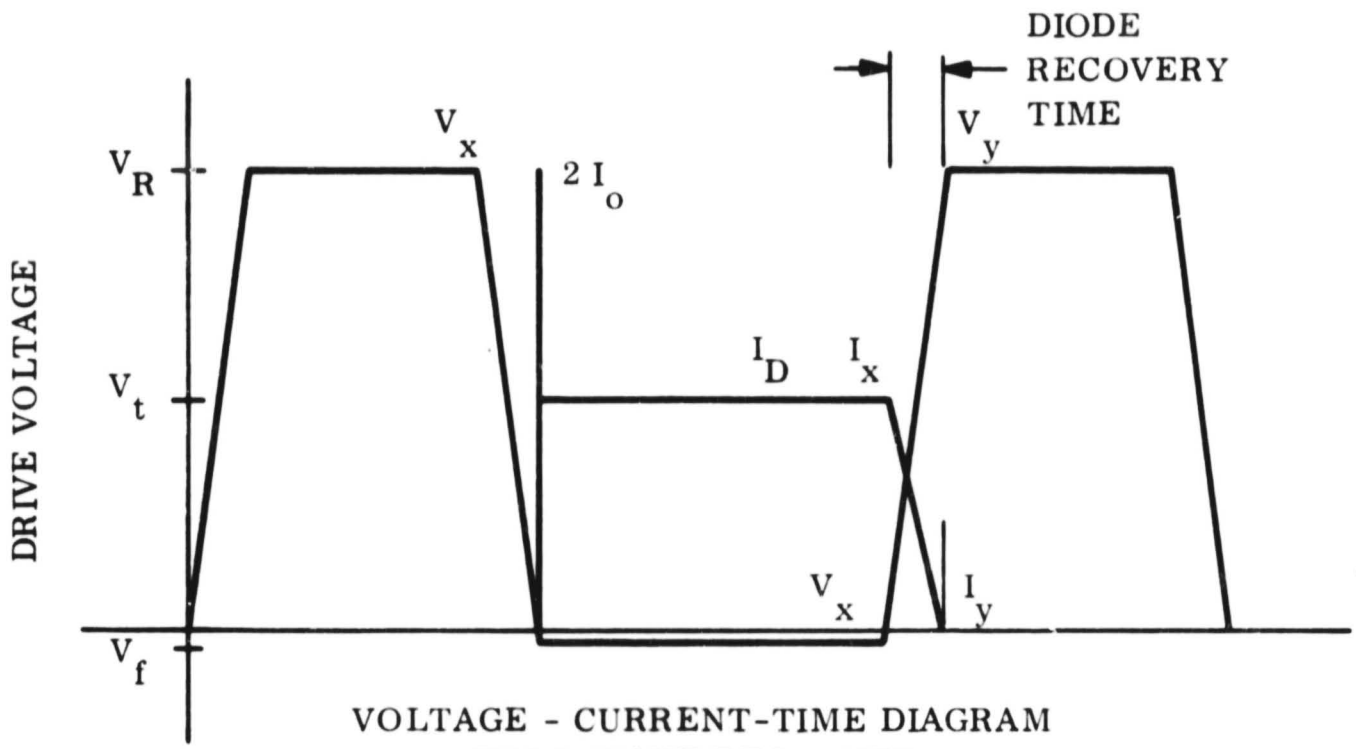
t_{rec} is recovery time of rectifier.

Total rectifier losses are

$$P_{total} = P_{forward} + 2P_f,$$

$$P_{total} = V_f I_d + 1/3\, f\, V_r I_d t_{rec},$$

where V_f is forward voltage drop.



VOLTAGE - CURRENT-TIME DIAGRAM
FULL-WAVE RECTIFIER
CHOKE INPUT FILTER

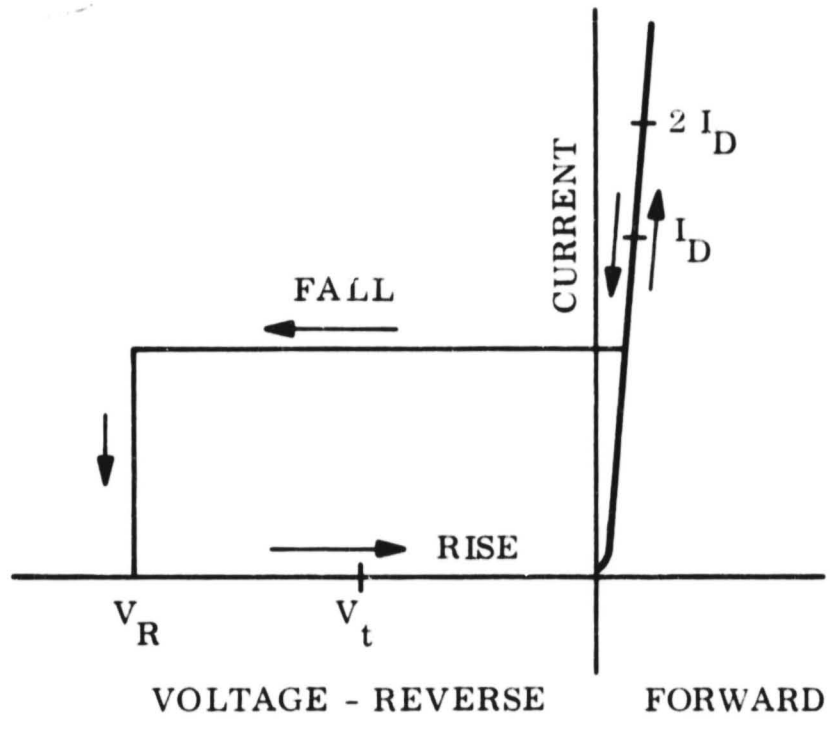


Figure 5.1.2-9 Rectifier Switching Characteristics

5.1.3 POWER SWITCHING AND DISTRIBUTION

This section discusses the present status of electrical equipment design in the power control, switching, and distribution areas of power system design as they midht relate to future Mariner spacecraft. The information presented here is based primarily on hardware experience with the Nimbus satellite, the Gravity Gradient Test Satellite, Biosatellite, and classified programs. All of these systems use dc distribution and the concepts discussed are applicable to such dc systems in general. The specific design characteristics to be discussed are:

- Flexibility to incorporate changes
- Command Input Redundancy
- Driver Failure Protection
- Command Matrix Implementation
- Noise Sensitivity
- Relay Coil Suppression
- Soft Commutation
- Contact Suppression

No specific recommendations are made at this time. However, detailed experimental and analytical evaluation of some of the concepts reviewed in this section should be undertaken in Phase II.

5.1.3.1 Flexibility

In the context of power switching and distribution design, flexibility pertains to the ease of incorporating changes which normally arise in the course of a hardware program.

Such flexibility has been attained by locating as many switching functions as possible within a single distribution unit including the provision for spares. The use of a single distribution unit has the advantage of concentrating switching and distribution design within one area of specilization and usually results in a more uniform selection of switching devices, more efficient packaging, and reduced noise susceptibility.

All power switching has been typically accomplished with standard latching and holding relay styles. Most applications can be accommodated with contact ratings of two or ten amperes. A long history of performance of these standard devices increases confidence in their use and also reduces replacement costs and simplifies logistics.

The practice has been to separately compartment the relays and relay drivers. Relays are insensitive to noise, require a significant energy pulse to activate the contacts, but are noise generators. The transistorized relay drivers are very sensitive to noise and are protected from relay transients by a separate enclosure. The wire carrying the relay coil signal can have noise induced on it between the transistor driver and the relay coil, but the coil will not respond to this low energy noise.

Spare relays are provided in the power control unit for flexibility and growth as the system evolves. All contacts are wired out to the electrical connector on the component, and multiple diode isolated lines are prewired to allow for redundant commanding. The spare relays are tested as part of the component acceptance and qualification test program, and thus are available in the vehicle to support required changes. The multiple use of similar relays in the component qualifies the new application without special attention to the previously unused relay.

The spare relays are made accessible to the system by changes in the vehicle distribution harness. The concept here is a rear-release crimp contact in the harness connector that allows wires to be switched from one termination point to another without cutting, splicing, soldering, or potting. The electrical connector is disassembled, the required change or additional wiring applied, and the connector reassembled. The changed hardness is revalidated by a full electrical functional test to assure that the required change meets the application. The change does not require that a component be recycled back to the wire shop, thru an electrical functional check, or thru a requalification cycle. The schedule impact on the vehicle flow cycle when the change is incorporated in the vehicle harness is in the order of four to twelve hours, depending on the complexity of the electrical functional test to verify and revalidate the harness.

The crimp contacts eliminate a requirement for skill, judgment, and competence on the part of the operator. The wire is cut and stripped of insulation to a calibrated length with an automatic hand operated tool, the contact is placed on the stripped end of the wire, and a calibrated crimping tool makes a metallurgical pressure bond between the wire and the contact. These tools are calibrated daily as they flow to and from the tool crib. The finished contact can be inspected after the operation is complete to insure that the wire protrudes past the crimp portion, that the indentations at the crimp section are of a sufficient but not excessive depth, and that the insulated portion of the wire extends sufficiently.

5.1.3.2 Command Input Redundancy

Protection against an open command line on an essential function can be designed into the hardware by providing two or more commands to the same relay coil from various coil drivers in the same or different sources. An example of this is a lock-stepped sequence with a timed command capability. Once the critical sequence is initiated, the initial and each subsequent command activates its own event and starts a separate timing circuit that will time out after the next command is due. If the command does not occur, the back-up timer activates the next event, and diode isolation prevents a fault in the command system from preventing the back-up timer from initiating the next event.

As shown on Figure 5.1.3-1 this concept provides protection against an open command line, but does tend to complicate the required vehicle wiring.

5.1.3.3 Driver Failure Protection

When it is necessary to protect against a shorted relay driver applying continuous power to a latching or holding relay, the protection can be provided by switching both ends of the relay coil. It should be noted that a shorted relay coil driver in a conventional system with a common ground return will prevent deactivation of either a latching or a holding relay. This is obvious in the case of the holding relay, and is also true for the latching relay, since the magnetomotive force generated by both the set and reset coil are essentially equal and in opposite directions. It is thus impossible to reset a latching relay when continuous power is

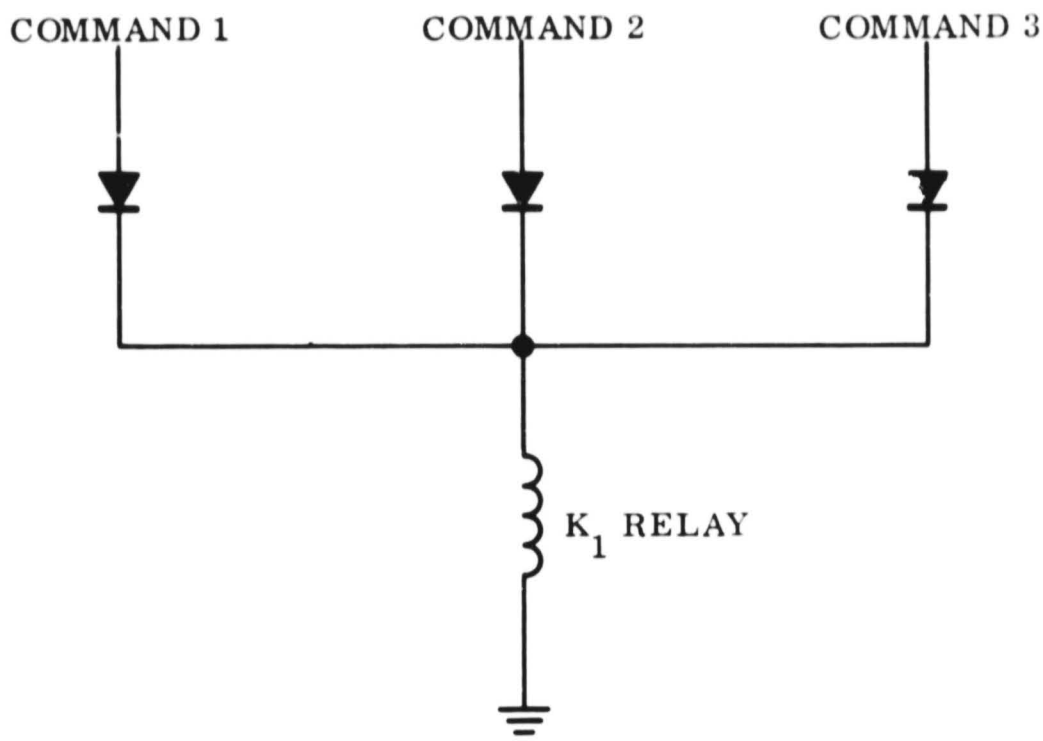


Figure 5.1.3-1. Redundant Commanding

being applied to the set coil. To activate an event it is then necessary to turn on positive power to the top of the coil and also provide a ground return for the bottom. Failure of either switch in a shorted position is insufficient to maintain power on the relay coil.

Figure 5.1.3-2 shows how protection is provided against a shorted command line on either the positive or ground side. Two failures are required to cause a malfunction of the relay.

5.1.3.4 Command Matrix Implementation

The driver failure protection described above at least doubles the amount of vehicle wiring. When power control is centrally located, the protection can be provided and the vehicle wiring can be reduced by using a matrix concept for relay activation as shown on Figure 5.1.3-3. When the X_1 command line is energized, nothing will occur until one of the three Y command lines is returned to ground. If command line Y_2 is returned to ground at the same time that the X_1 command line is energized, then relay coil K_{12} will be activated, but no other relay.

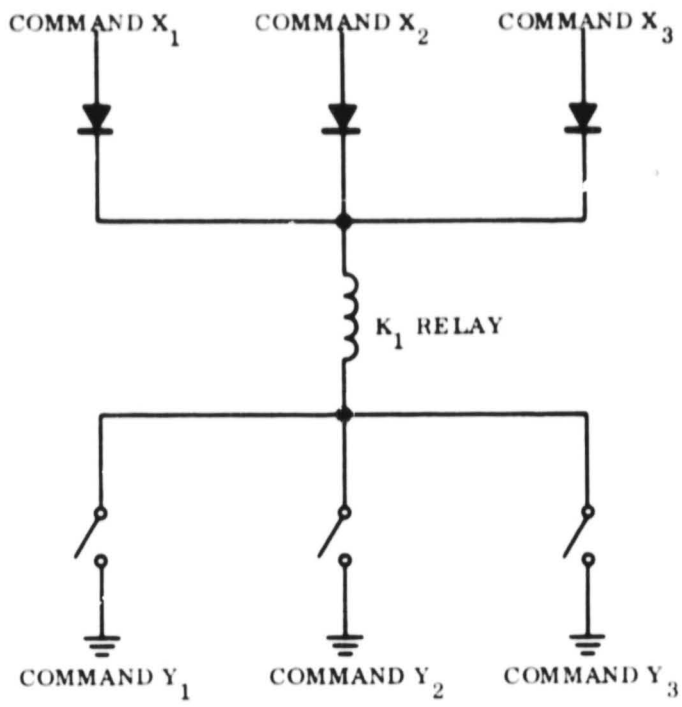


Figure 5.1.3-2. Driver Failure Protection

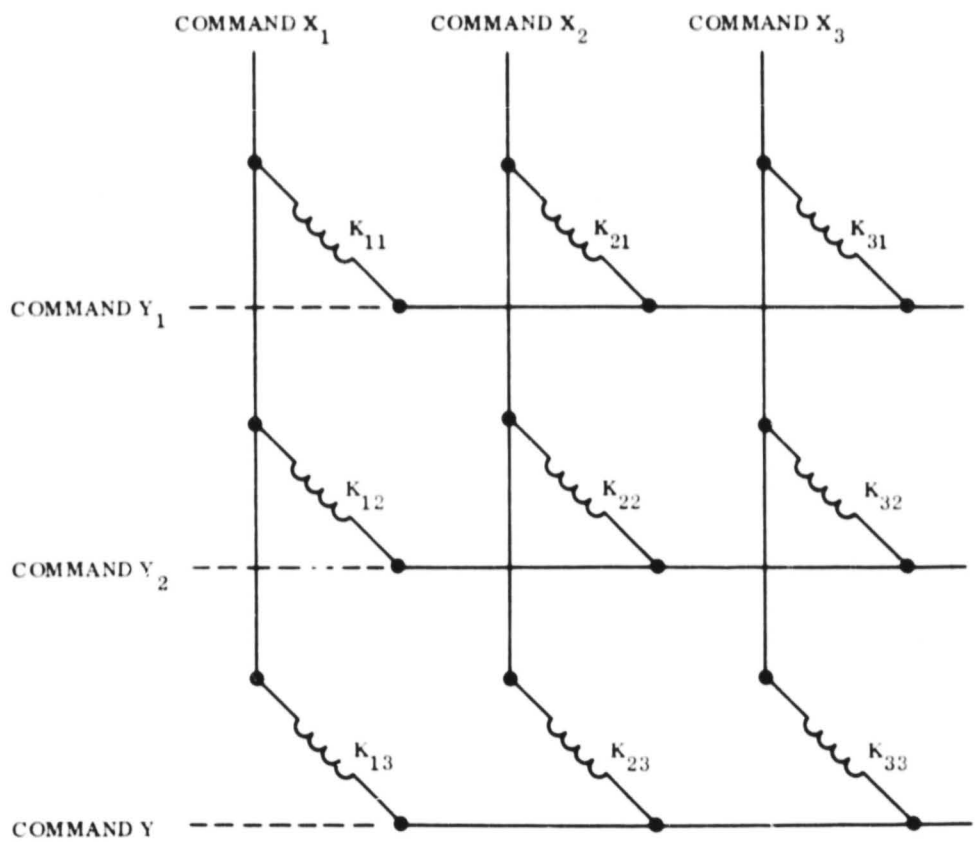


Figure 5.1.3-3. Simplified Command Matrix

This concept allows n^2 events to be commanded with 2n separate commands when the commands are arranged in a square array as shown. At least two failures are required before a malfunction occurs. However, if any one command line fails, two events will occur whenever a command is issued. The desired event will occur, and at the same time the valid command will complete the circuit for the failed command line, and allow that event to occur also. It is relatively easy to verify the failure, and a contingent mode capability would allow all subsequent command lists to reset the undesired event immediately after a valid command completed the circuit for a failed command line.

5.1.3.5 Noise Sensitivity

When a relay is to be activated, sufficient energy must be supplied in the form of an electrical pulse to establish a magnetic field sufficient to overcome a spring force restraining the moving contact. Electromagnetic relays are relatively insensitive to noise, since a pulse of a significant magnitude and duration is required to accomplish the event. Figure 5.1.3-4 shows a typical relay characteristic for a coil rated for twelve-volt service used in a twenty-eight volt system.

The transistorized relay driver is an active amplifier, and will act on a noise pulse of the proper polarity thru the gain of the transistor to possibly cause problems. These problems are minimized by locating the relay drivers in a relatively quiet region remote from the relays. The relays are extremely noisy and would cause the relay drivers to react in a detrimental fashion. However, the relays can exist in their own environment and are insensitive to their own noise.

5.1.3.6. Relay Coil Suppression

When the current through an inductive circuit is interrupted, a large potential may appear at the terminals of the inductor. The energy stored in an inductor because of a steady-state current must be dissipated before the current goes to zero. When the coil is driven by a semiconductor switch, the energy may destroy the switch if not controlled. A simple

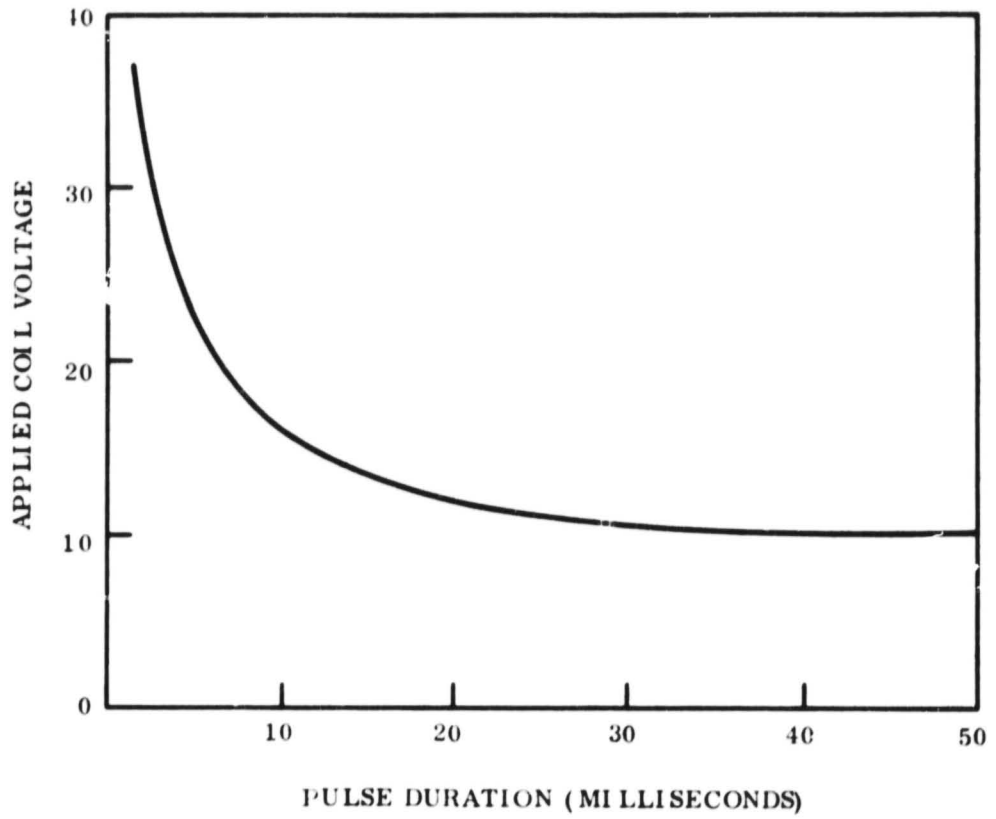


Figure 5.1.3-4. Relays Insensitive to Noise

protection method uses a conventional diode suppression circuit where the induced voltage forward biases a diode to provide a current path as shown on Figure 5.1.3-5.

The turn-off transient can be more effectively controlled by replacing the switch with an active circuit capable of supplying to the coil a current with diminishing magnitude. The rate of change of current may then be constrained to values low enough to avoid induced voltages. In Figure 5.1.3-5 the transistor traverses the active region at a slow rate, and the only consequence is an increase in the pull-in and drop-out times of the relay.

5.1.3.7 Soft Commutation

Of special interest in power control is the radiated field generated when current changes in a vehicle harness wire. To limit these fields to acceptable levels, it is necessary to control the rate of current rise or fall to values in the order of 5000 amperes per second. This can be accomplished by providing line inductance, or by controlling the rate of change of current with semiconductor switches. Figure 5.1.3-6 illustrates these approaches.

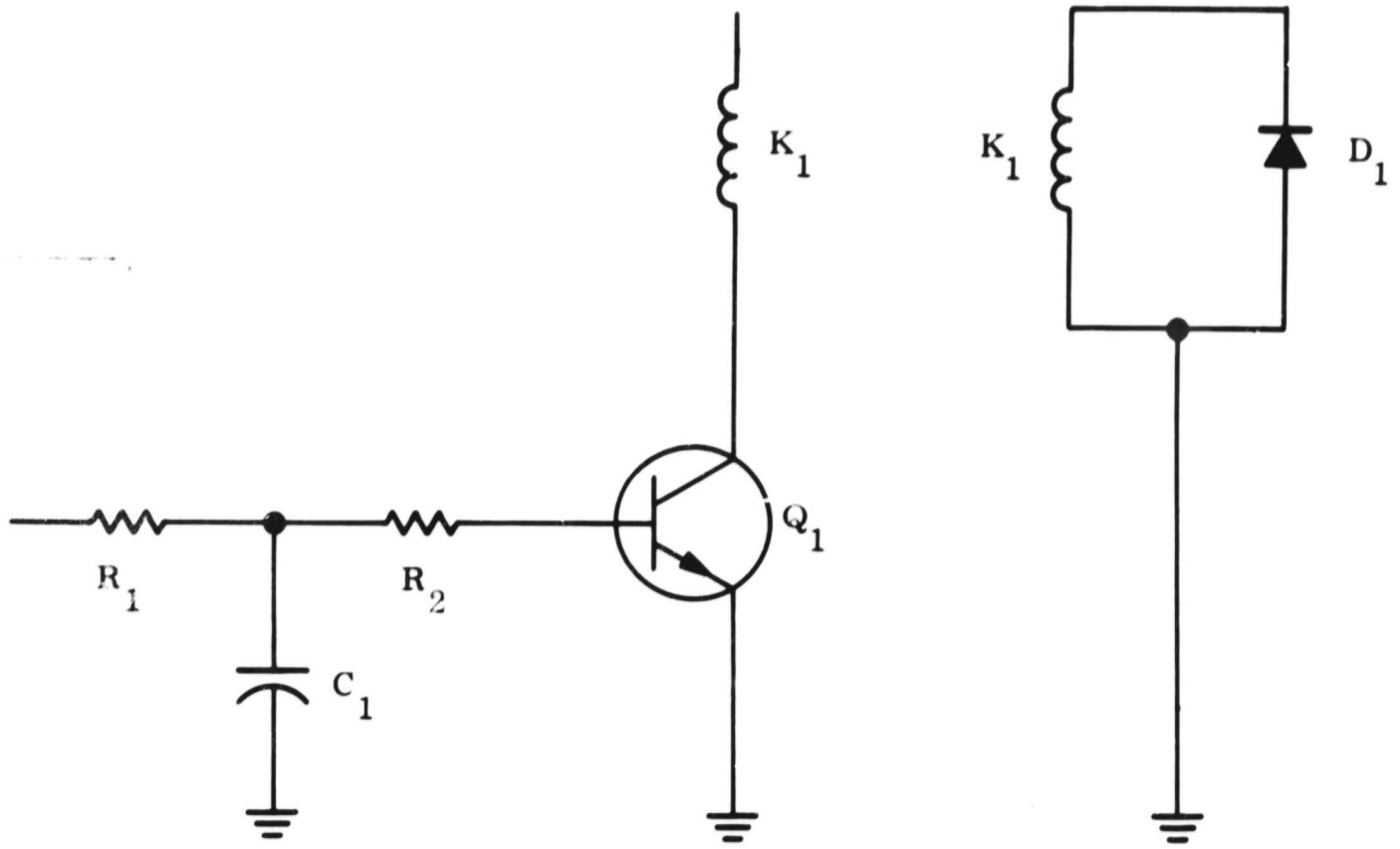


Figure 5.1.3-5. Coil Suppression

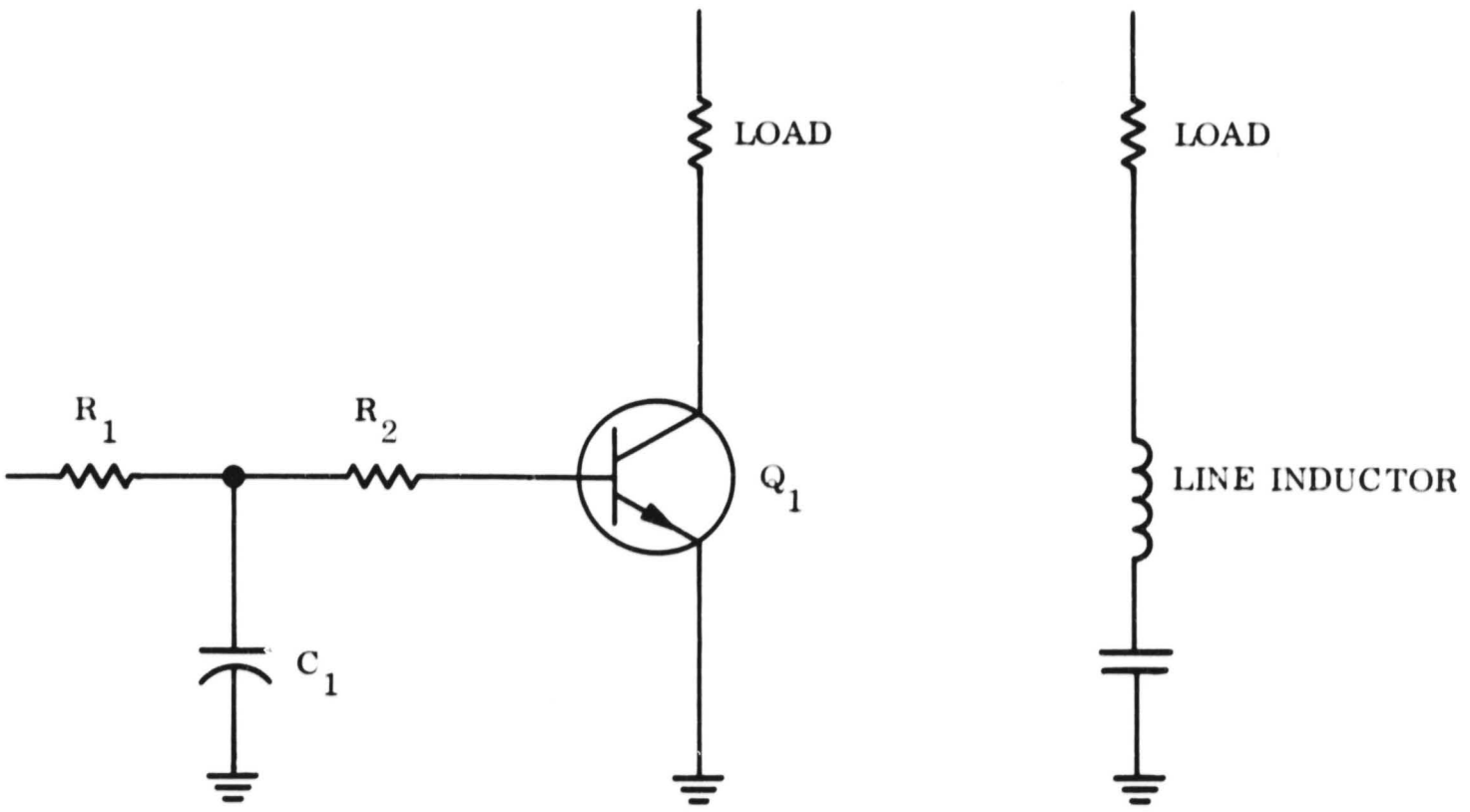


Figure 5.1.3-6. Soft Commutation

5.1.3.8 Contact Suppression

An inductive load will not allow current to change instantaneously, and when a relay contact attempts to interrupt such current flow an arc is established. The duration of the electromagnetic noise generated is increased by coil suppression, since the drop-out time increases, and is also increased if the load is deliberately made inductive to control the rate of current rise at turn-on.

The arc suppression problem can be solved by a resistance-diode-capacitance network across the relay contacts as shown on Figure 5.1.3-7. The rapid voltage rise at contact opening is caused by the inductive load keeping the load current essentially constant. This current, on contact opening, is fed from the distributed capacity of the circuit wiring. As the voltage rises, at some value of voltage, arcing will occur across the contacts, discharging the wiring capacity. If the load inductance is large, the load current will not have decreased appreciably, and the process will be sustained at an increasing value of breakdown voltage since the contact gap will have increased.

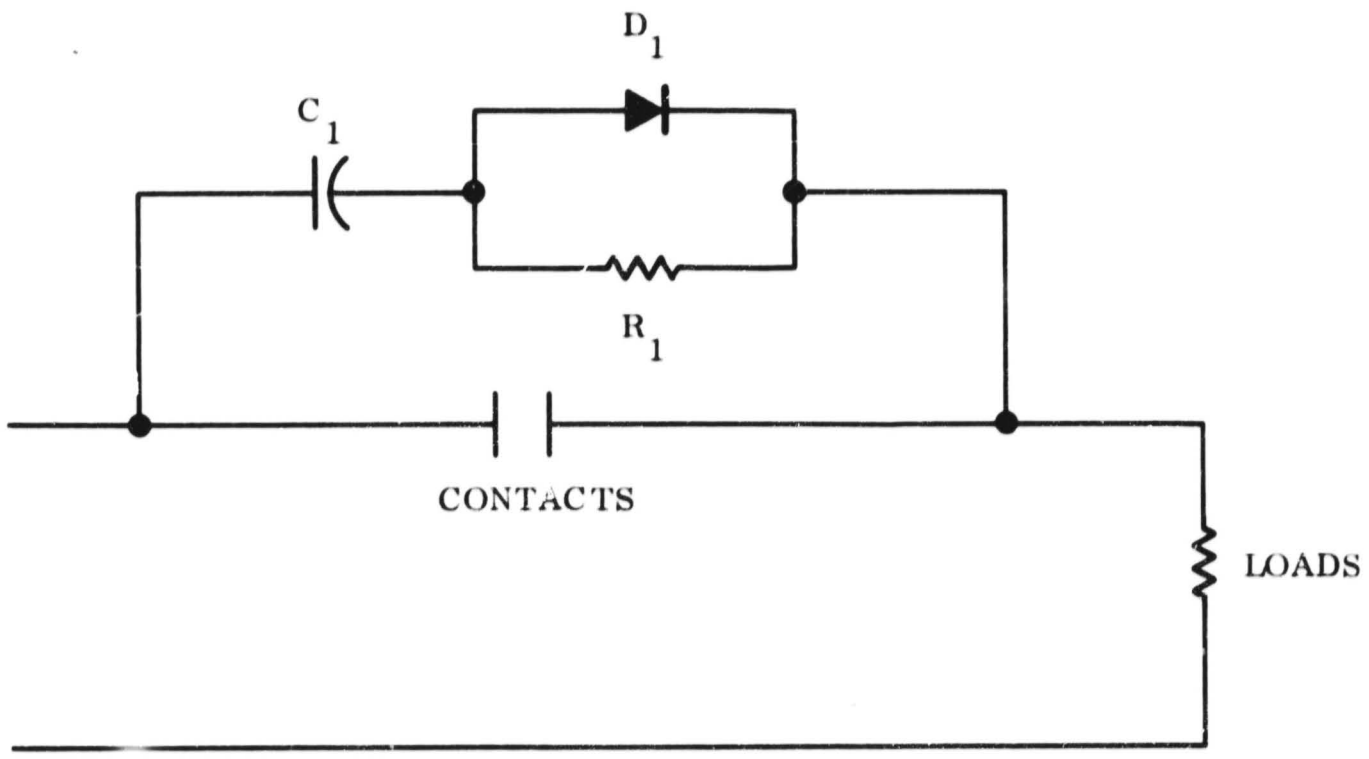


Figure 5.1.3-7. Contact Suppression

The value of capacity to be furnished must be sized to limit the arc-over voltage. Its size is a function of the load current and the opening time of the contacts.

$$C = \frac{It}{V}$$

where: C = Capacitance required in farads

I = Load current in amperes

t = Opening time in seconds (to any gap value)

V = Gap breakdown at any spacing in volts

Just prior to contact closure this capacitor is charged to the bus voltage that has been across the open contacts. When the contacts close, this capacitor is short-circuited across the contacts, causing excessive surge currents and rapid contact deterioration. This reclosure surge can be controlled by a resistor in series with the capacitor to limit the surge current to a safe value. A good approximation is to make this resistance equal to the load resistance. The load current will increase from zero because of the inductive load, and the surge current will decrease from its initial value due to the CR time constant.

The series resistance destroys the capacitor's effectiveness to furnish the current when the contacts open, but this defect can be corrected by shorting the resistor with a diode. The series resistance for surge protection on contact closure is still retained.

Information required to size the arc suppression circuit is:

a. Equivalent series inductance of the load
b. Equivalent series resistance of the load
c. Distributed shunt capacitance of wiring between contacts and the load
d. Contact closure time, maximum at worst case

Preliminary experimental evidence indicates that arc-over occurs at some low value of voltage before any significant gap has been achieved, and that this arc is maintained at

15 volts or less during an opening time of two milliseconds. The capacity would have to furnish load current to prevent this voltage from appearing across the contacts. The phenomenon apparently is controllable only by the rate of voltage rise across the contacts. A minimum value of capacity would then appear to be:

$$C = I_{LOAD} \times \frac{1}{\frac{DV}{Dt}}$$

where $\frac{DV}{Dt}$ is the maximum voltage rise that will not ignite the arc. It is on the order of one volt/microsecond, making:

$$C = I_{LOAD} \text{ microfarads}$$

5.1.4 PCU FAILURE DETECTION

5.1.4.1 Fault Sensing Criteria

The concept of replacing a faulty power conditioning unit (PCU) with a standby unit implies that measurement of the original unit against a set of performance criteria is necessary. Figure 5.1.4-1 shows the functions of a fault detector based on such criteria for transferring operation to the standby unit. This section considers and defines such criteria for representative types of PCU's.

Any particular PCU has a defined functional requirement for a given set of external conditions. For example, a series dissipative voltage regulator is required to deliver power within a specified voltage tolerance providing the input power is available within a certain voltage range and providing the output load is within certain limits. If these external operating conditions are satisfied, the regulator requirements themselves serve as the criteria for proper unit operation. Thus, in the case of the series voltage regulator, the delivery of power within a specified voltage range serves as the fault sensing criterion providing the other external conditions are satisfied. A broader set of criteria must, however, be postulated to cover those situations where the external conditions are not satisfied. The series regulator, for example, cannot be expected to function normally if the input voltage is too low. Under this condition, the fault sensing criterion based on normal input conditions would have indicated a failed regulator. Thus, the general definition of fault sensing criteria must consider both normal and abnormal external conditions.

There are several ways for attacking this general problem. First, the behavior of a properly functioning PCU can be studied for the entire range of normal and abnormal external conditions, and the results, either analytical or experimental, used to establish fault sensing criteria. Consider again the series voltage regulator. If the input voltage is too low, a properly functioning series regulator will simply produce the input voltage at its output with some deviation depending on the load. By varying the input voltage over its entire abnormal range, the PCU behavior (specifically the output voltage variation), can be mapped for different load conditions. The resulting mapping function can be considered as an

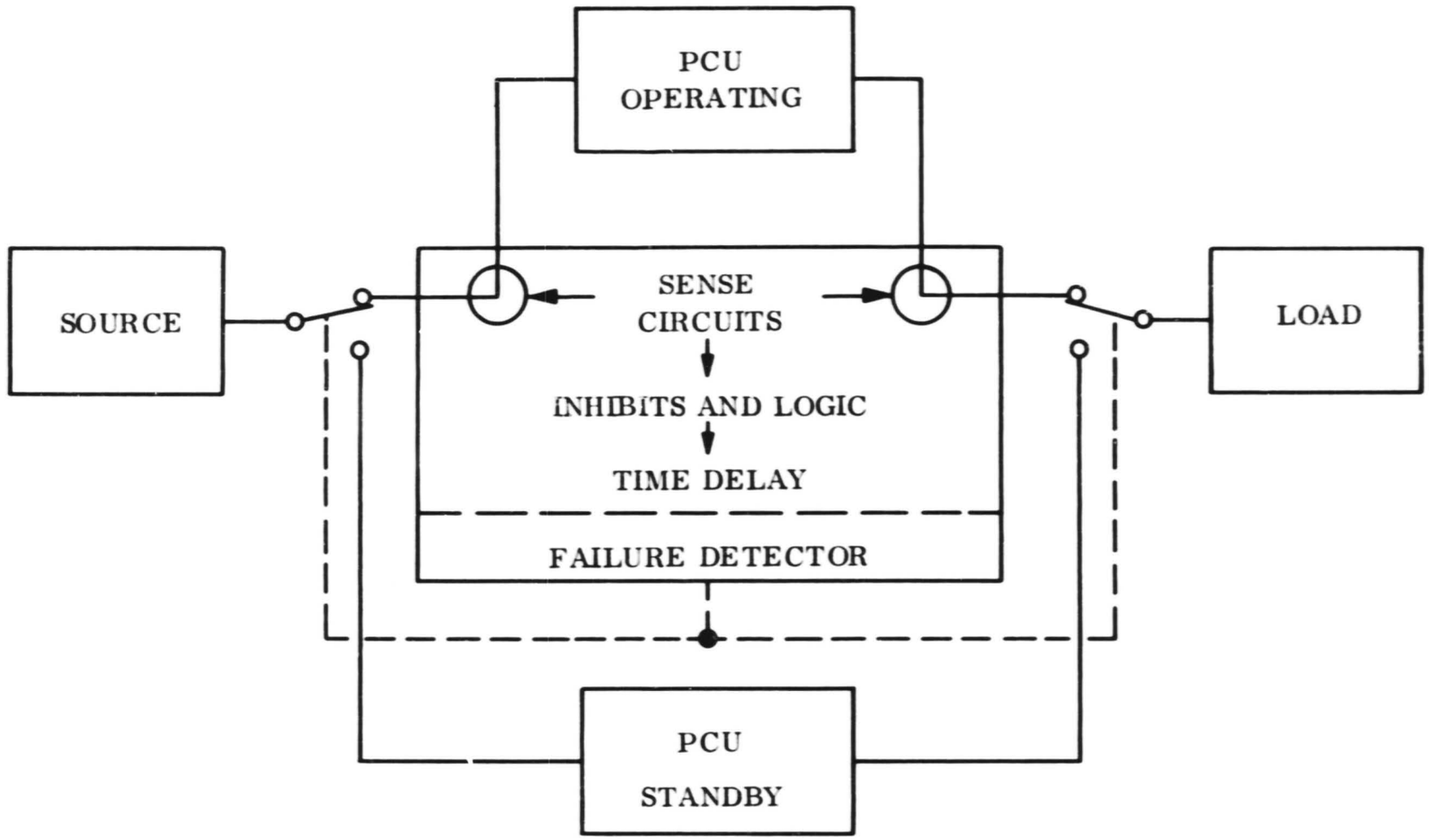


Figure 5.1.4-1. System Block Diagram

analog model representative of proper operation of the PCU. Conceptually, this model could serve as the basis for fault sensing criteria, i.e., in an actual mechanization the behavior of the operating PCU would be compared to the analog model. Practically, of course, this approach is difficult to implement. It would probably be complicated because of the implied computer functions, and the mapping function might be difficult to predict, duplicate, and verify.

A second more practical way of considering normal and abnormal external conditions is to recognize the abnormal conditions and avoid comparisons during such periods. For example, if load on a PCU is excessive, its corresponding low output voltage would be ignored as a criterion of failure. The definition of such inhibit functions is not always obvious and must be examined carefully for each PCU type. For example, a low input voltage to the series regulator could have been caused by failure of the regulator and a fault sensing inhibit would not be desirable.

The second approach has been adopted in examining the fault sensing criteria for the following typical PCU's:

a. Series dissipative regulator

b. Inverter or converter

c. Switching regulator (buck, boost, etc.)

d. Shunt regulator

Table 5.1.4-1 summarizes the fault sensing criteria and inhibit functions for these PCU's in accordance with the nomenclature shown. As indicated for the first criterion, the table should read as follows: "Faiiure indicated when $V_o > V_{RMAX}$ except if $V_I > V_{IMAX}$ or $I_o < I_{oMIN}$".

The following sections provide more detailed discussion on each PCU type.

Table 5.1.4-1. Fault Criteria Summary

PCU Type	Failure Criteria	Inhibit Zones
Series dissipative regulator	Failure indicated when $V_O > V_{RMAX}$	except if $V_I > V_{IMAX}$ or $I_O < I_{OMIN}$
	$V_O < V_{RMIN}$	$V_I < V_{IMIN}$ or $I_O > I_{OMAX}$
	$I_O < I_I$	$I_I < I_{IMIN}$
Inverter, Converter	$V_O \neq K_1 V_I$	$V_I < V_{IMIN}$ $I_O > I_{OMAX}$
	$I_O \neq K_2 I_I$	$I_I < I_{IMIN}$
Switching Regulator	$V_O > V_{RMAX}$	$V_I > V_{IMAX}$ or $I_O < I_{OMIN}$
	$V_O < V_{RMIN}$	$V_I < V_{IMIN}$ or $I_O > I_{OMAX}$
	$P_O < \eta_{MIN} P_I$	$I_O < I_{OMIN}$ or $I_O > I_{OMAX}$ or $I_I < I_{IMIN}$
Shunt Regulator	$V_O > V_{RMAX}$	$I_S (= I_I - I_O) > I_{SMAX}$
	$V_O < V_{RMIN}$	$I_S (= I_I - I_O) < I_{SMIN}$

Nomenclature:

I	Current
V	Voltage
P	Power
η	Efficiency, output power/input power
K	Arbitrary constant

Subscripts:

I	Input
O	Output
R	Regulated
S	Shunt
_MAX	Maximum value of previous subscript Ex. V_{OMAX} = maximum output voltage
_MIN	Minimum value of previous subscript
1, 2, ...	Arbitrary designations

5.1.4.1.1 Series Dissipative Regulator

The series dissipative regulator is described by the three curves of Figure 5.1.4-2. Their relation with each criterion of Table 5.1.4-1 is as follows:

a. $V_O > V_{RMAX}$: Curve A shows the relationship of V_I and V_O. V_O follows V_I up to a certain minimum value (V_{IMIN}) and remains constant until some maximum allowable value of V_I (V_{IMAX}). Thereafter V_O increases accounting for the inhibit function $V_I > V_{IMAX}$. Curve C shows the relationship of V_O and I_O. At very low values of I_O, V_O can increase above the regulation limits accounting for the inhibit $I_O < I_{OMIN}$. For series dissipative regulators, I_{OMIN} is practically zero, and therefore, the possible rise in V_O is not shown.

b. $V_O < V_{RMIN}$: The inhibit function $V_I < V_{IMIN}$ follows from curve A when $V_O \approx V_I$ up to the point where $V_I = V_{IMIN}$. Curve C shows a drooping output for $I_O > I_{OMAX}$ accounting for this second inhibit.

c. $I_O < I_I$: In a series dissipative regulator, the input current is equal to the output current for all conditions with appreciable inequality only at very low loads as shown on curve C. The appropriate inhibit function is, therefore, $I_I < I_{IMIN}$.

5.1.4.1.2 Inverter or Converter

Inverters or converters are described by the three curves of Figure 5.1.4-3. Their relation with the criteria described in Table 5.1.4-1 are as follows:

a. $V_O \neq K_1 V_I$: Since inverters and converters are strictly voltage transformation devices, the voltage ratio shown by curve A is constant providing V_I is greater than some V_{IMIN} (usually about 10 volts determined by switch voltage efficiency). Normal performance is expected as long as V_I is above V_{IMIN} as shown by curve A and C. Curve C also shows that with $I_O > I_{OMAX}$, V_O decreases causing the ratio $V_O/V_I \neq K$; however, a transfer is inhibited because $I_O > I_{OMAX}$ is an overload. Therefore, an output voltage failure is indicated when $V_O \neq K_1 V_I$, except for inhibit conditions of $V_I < V_{IMIN}$ and $I_O > I_{OMAX}$.

b. $I_O \neq K_2 I_I$: Curve B shows the input current, V_I, as a function of load current, I_O. This ratio under normal performance is constant above I_{IMIN} (established by fixed losses of PCU). If I_I rises due to additional internal losses, then $I_O \neq K_2 I_I$ and the PCU is failed, except if $I_I < I_{IMIN}$. If $I_O \neq K_2 I_I$ and $I_I > I_{IMIN}$, the PCU is failed.

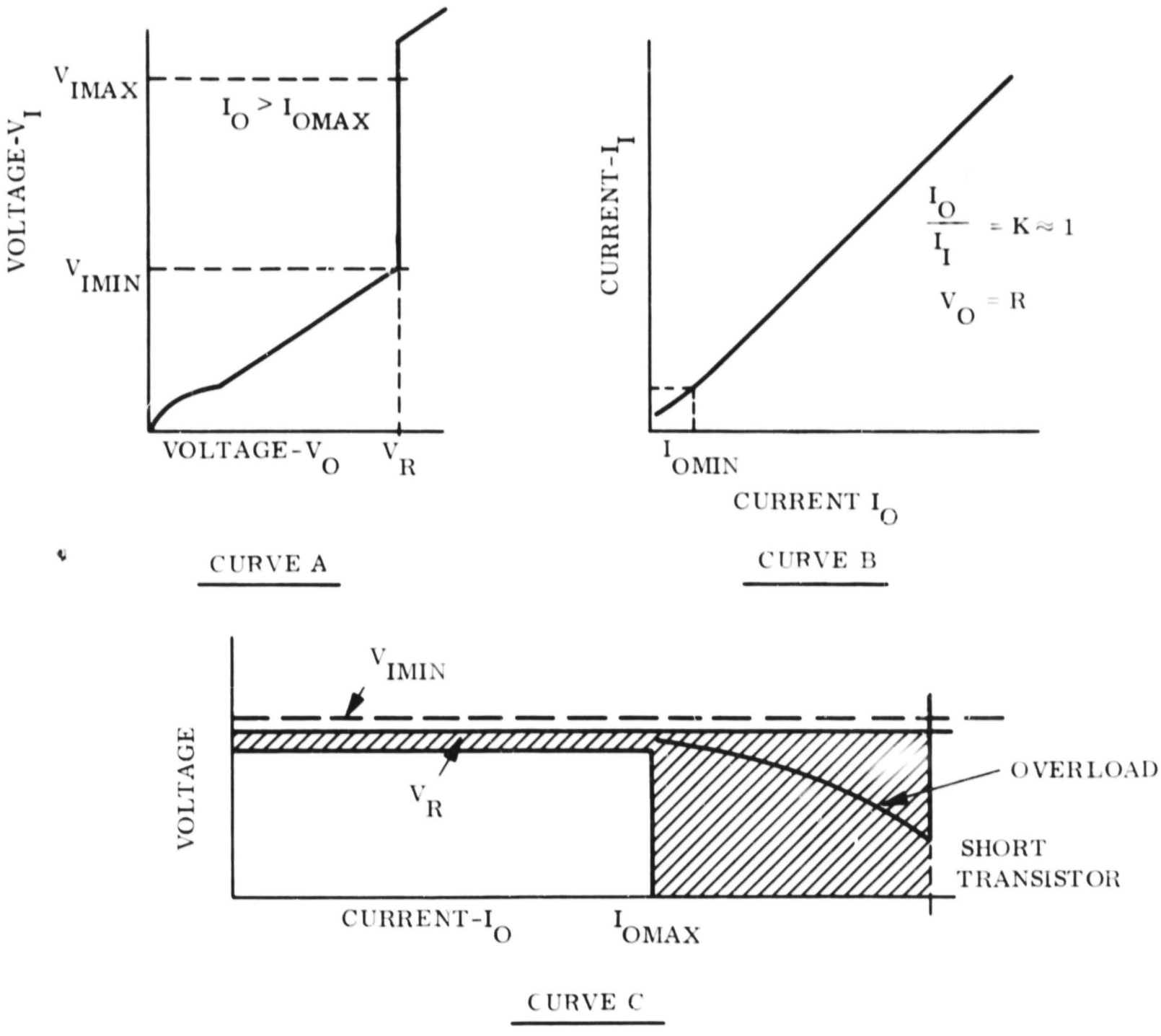


Figure 5.1.4-2. Voltage - Current Characteristics of Series Dissipative Regulator

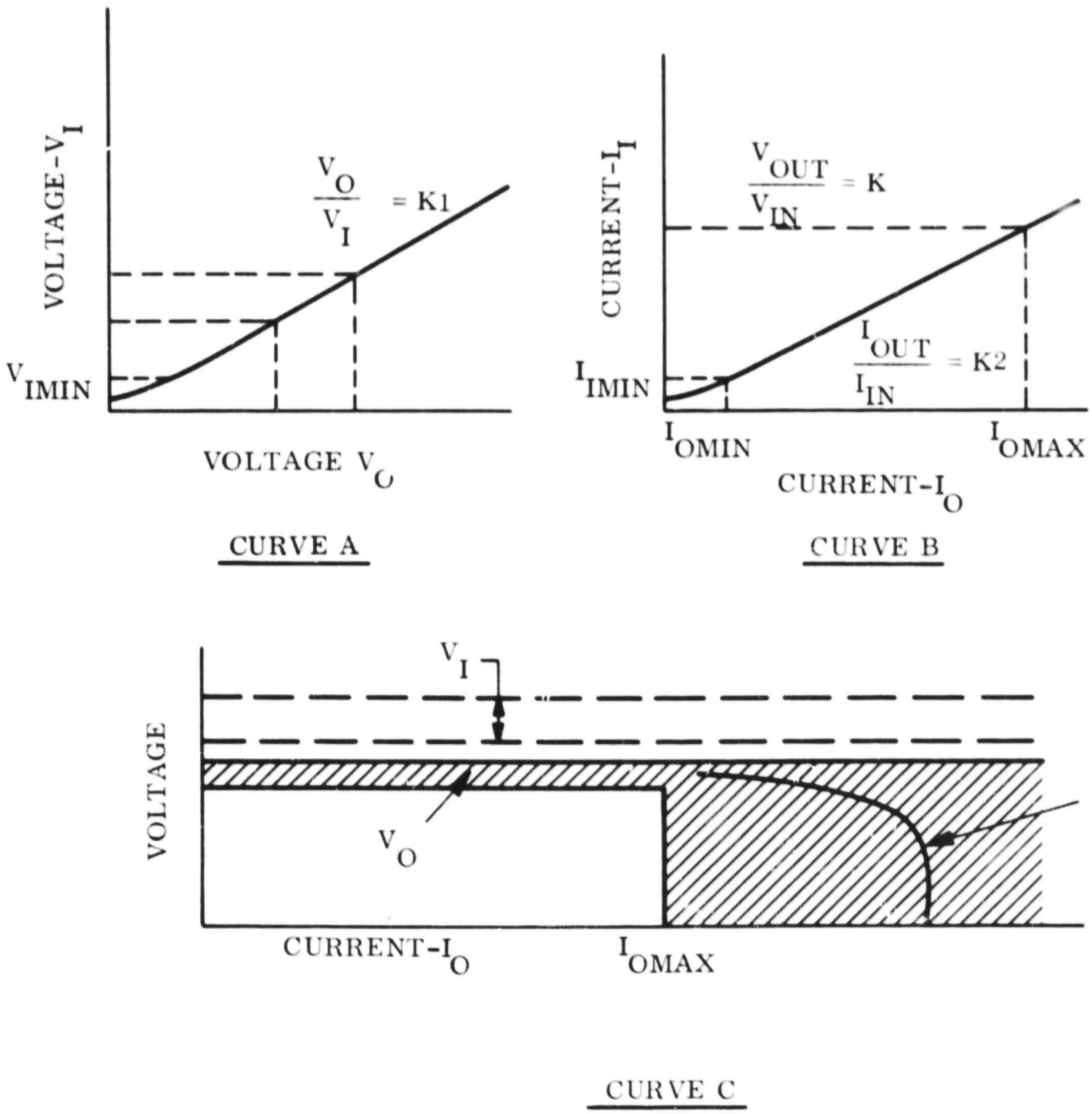


Figure 5.1.4-3. Voltage - Current Characteristics of Inverter or Converter

5.1.4.1.3 Switching Regulators

The switching regulator is described by the three curves of Figure 5.1.4-4. These curves describe the general characteristics of buck, boost, buck-boost and converter or inverter/regulator combinations with a single critical output. Their relation with the criteria described in Table 5.1.4-1 are as follows:

a. $V_O > V_{RMAX}$: Curve A shows the relationship between V_I and V_O. This curve is similar to the series dissipative regulator V_I V_O curve, except V_O may be greater or less than V_I. Curve A shows that $V_O > V_{RMAX}$ when $V_I > V_{IMAX}$; therefore, the PCU is failed when $V_O > V_{RMAX}$, except if $V_I > V_{IMAX}$. Curve C shows that $V_O > V_{RMAX}$ if $I_O < I_{OMIN}$ (a characteristic of the LC output filter under light loads). Therefore, the PCU is failed when $V_O > V_{RMAX}$, except if $I_O < I_{OMIN}$.

b. $V_O < V_{RMIN}$: Curve A shows that $V_O < V_{RMIN}$ when $V_I < V_{IMIN}$ and Curve C shows that $V_O < V_{RMIN}$ when $I_O > I_{OMAX}$. Therefore, the PCU is failed when $V_O < V_{RMIN}$, except when $V_I < V_{IMIN}$ and $I_O > I_{OMAX}$.

c. $P_O < \eta_{MIN} P_I$: Curve C shows that between I_{OMIN} and I_{OMAX}, V_O is within regulation limits and the efficiency is reasonably constant and greater than η_{MIN}. If $P_O < \eta_{MIN} P_I$ the PCU is failed, except if $I_O < I_{OMIN}$ and $I_O > I_{OMAX}$. It is possible to have an efficiency failure when $I_O < I_{OMIN}$. Curve B shows that for $I_O = I_{OMIN}$, there is a $I_I = I_{IMIN}$. If $P_O < \eta_{MIN} P_I$, the PCU is failed if $I_I > I_{IMIN}$ or not failed if $I_I < I_{IMIN}$.

5.1.4.1.4 Shunt Regulator

The shunt regulator is described by the curve of Figure 5.1.4-5. Its relations with each criterion of Table 5.1.4-1 is as follows:

a. $V_O > V_{RMAX}$: At $V_O = V_{RMAX}$, the regulator is shunting maximum design current. For higher shunt current, it cannot maintain regulation, and therefore, the inhibit function is $I_S > I_{SMAX}$.

b. $V_O < V_{RMIN}$: At $V_O = V_{RMIN}$ the regulator normally shunts minimum current. If $I_S > I_{SMIN}$ when $V_O < V_{RMIN}$, the regulator is considered failed since I_S should be < I_{SMIN}. Therefore, the failure indication is $V_O < V_{RMIN}$, except if $I_S < I_{SMIN}$.

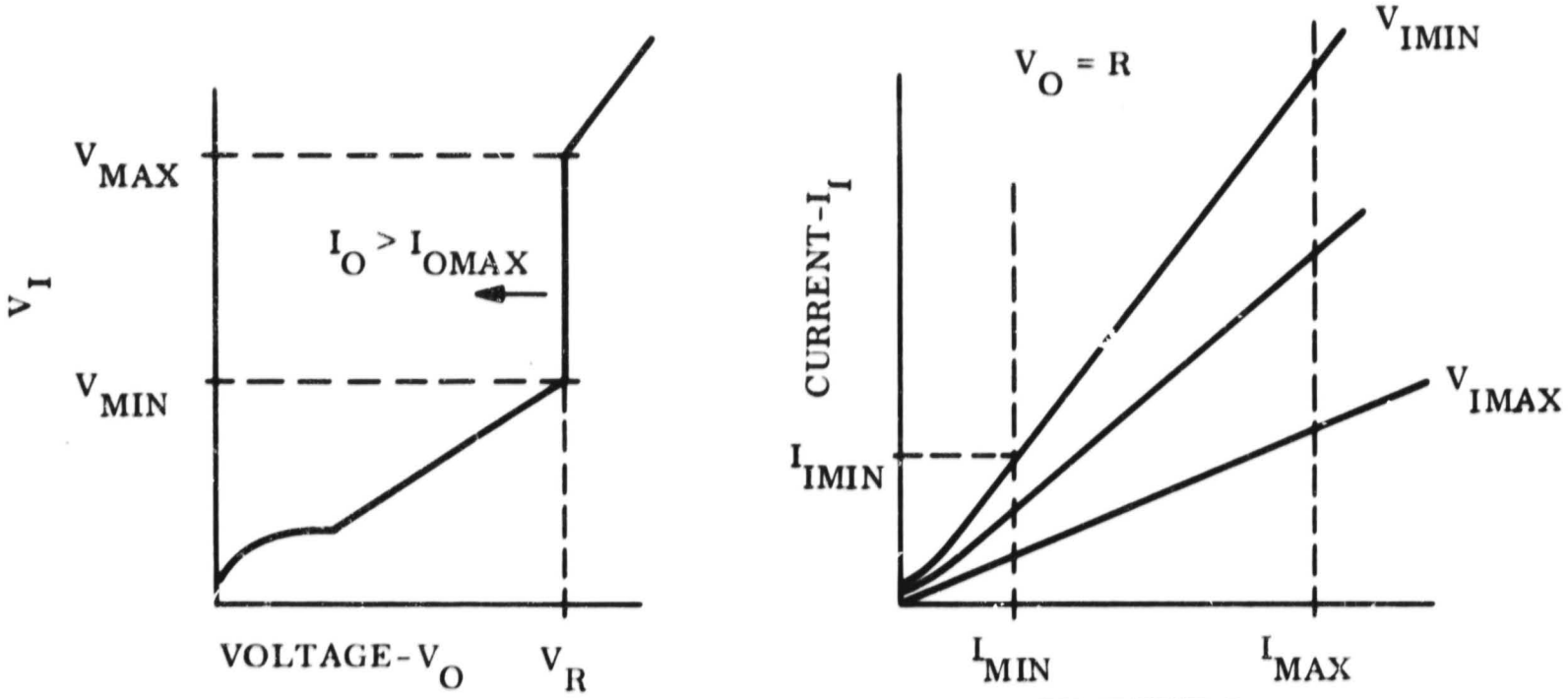


Figure 5.1.4-4. Voltage - Current Characteristics of Switching Regulator

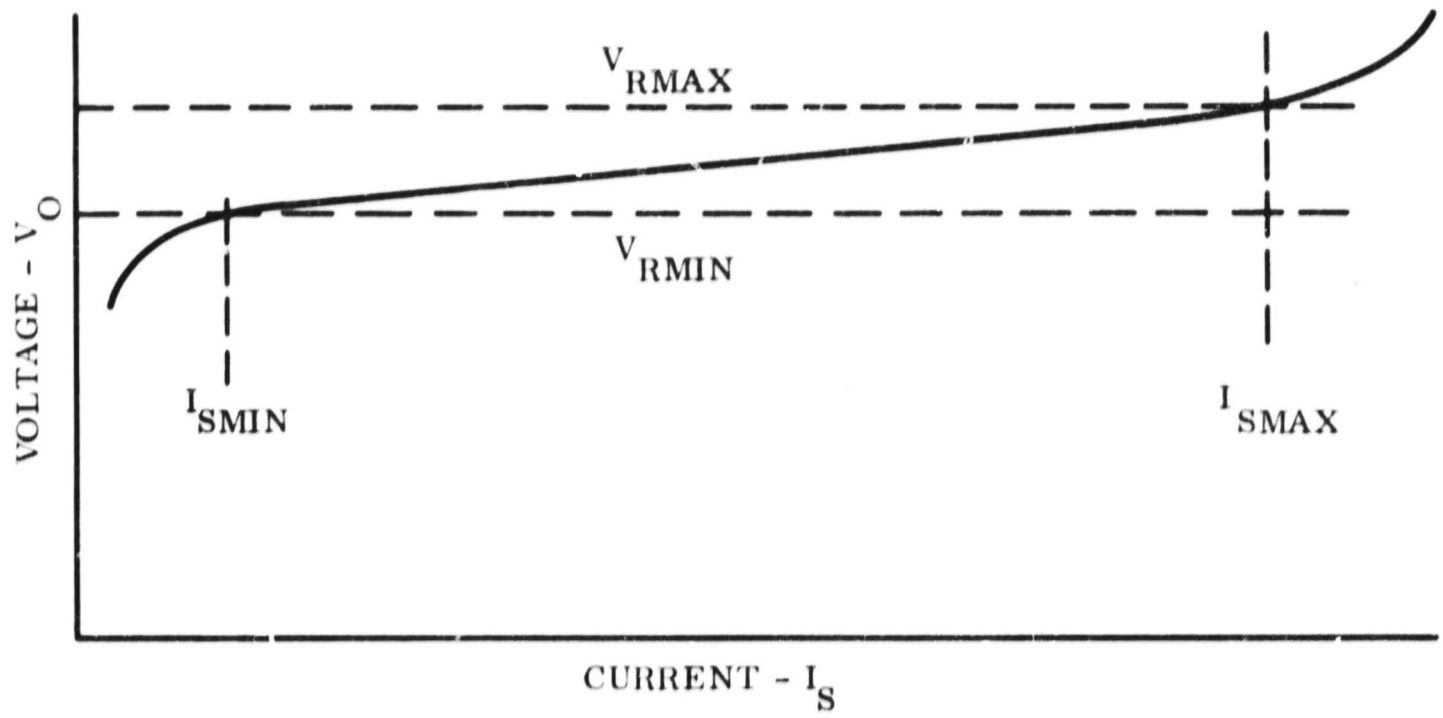


Figure 5.1.4-5. Shunt Regulator Characteristics

5.1.4.1.5 Discussion

In the failure column of Table 5.1.4-1, the defined failures for each PCU include output voltage deviations beyond some predetermined limit, e.g., $V_o < V_{oMIN}$ or $V_o > V_{oMAX}$. Within the context of voltage sensors is the special case of a frequency measurement through a tuned filter where if a frequency shift occurred the filter output voltage decreases. The other indications of failure shown in the table are:

$I_o < I_I$ for the series dissipative regulator,

$I_o \neq K_2 I_I$ for the inverter or converter,

$P_o < \eta_{MIN} P_I$ for the switching regulator.

These relate to a decrease in efficiency for the particular PCU.

For the series dissipative regulator, the input current nearly equals the output current, except for some small control losses. If I_I becomes significantly greater than I_o, the internal losses have increased, with a corresponding efficiency decrease. For the inverter or converter, the output current is a fixed ratio to input current. (This is also true of the output to input voltage.) The ratio can only change if a fault occurs in a series switching element or in the transforming device. If an internal fault occurs the ratio changes, and internal losses have increased and an efficiency decrease has occurred. For the switching regulator, the efficiency is defined as the ratio P_o/P_I. If this ratio is less than some value, an efficiency decrease has occurred.

For the PCU's considered, it may be seen that the only failure indicators are output voltage deviation and efficiency decrease. Of all the failure detector requirements discussed, the failure detector for the switching regulator requires the greatest number of circuit functions (refer to Table 5.1.4-2). Note that the circuit functions required for any of the other failure detectors is included in the switching regulator failure detector which is easily modified for use with the other PCU's discussed.

The above fault sensing criteria pertain to steady-state behavior. During normal operation, transient conditions will occur causing the output voltage and efficiency to deviate from normal ranges. To distinguish between steady-state and transient deviations, it is necessary to incorporate appropriate time delay criteria.

5.1.4.2 Fault Sensor Requirements

The previous section established that PCU performance can be characterized by input and output parameters, and that deviations can be identified from these measured parameters. The next important step is to establish practical limits for fault detection pertaining to the voltage, efficiency, and time parameters discussed previously.

5.1.4.2.1 Voltage Limits

Fault detector tolerances associated with measuring under or overvoltage conditions must be added to the specified regulator tolerance to determine overall regulation limits. As an

Table 5.1.4-2. Diagnostic Circuit Summation for Relative Complexity

PCU	Series Dissipative Regulator		Converter or Inverter		Switching Regulator		Shunt Regulator	
Failure Indicators	Vout	Eff.	Vout	Eff.	Vout	Eff.	Vout	Eff.
	2-volt divider	2-curr 1-curr ratio	2-volt divider 1-volt ratio	2 curr 1 curr ratio	2 volt divider	2 curr 2 volt 2 (mult.) 1-power ratio	2 volt divider	1 curr
Load Inhibit	2 current		2 current		2 current		2 current	
Source Inhibit	2 voltage		1 voltage 1 current		2 voltage 1 current		None	
Circuit Summation	9		9		14		5	
Logic Circuits	-		-		Highest		Lowest	
					Most Complex Failure Detector			

illustration, practical voltage regulators might be specified with a 2 percent range of regulation. A voltage deviation fault detector, designed and built with the same degree of circuit sophistication, will have similar tolerances. These tolerances must not overlap the range for which the basic regulator is designed, and therefore, the net regulation range may be as high as 6 percent (adding 2 percent on either side of the regulator range) before a fault transfer is initiated. It is possible, of course, to reduce the detector tolerance through the use of more accurate circuitry, but nevertheless, the use of fault detectors will always result in an increased user regulation range as compared to the regulator range. Thus, an important distinction between block redundant and nonredundant systems, both employing similar types of equipment, is that the block redundant system will have a wider output tolerance. From practical laboratory experience, voltage fault detectors can be designed without difficulty with a tolerance of 0.5 percent. This would incur an additional tolerance in overall regulation of 1 percent considering both under and overvoltage detectors.

5.1.4.2.2 Efficiency Limits

The detection of a decrease in PCU efficiency has the principal purposes of: (a) conserving power and energy margins of the system, and (b) avoiding damage to other spacecraft equipment which may result from the increased thermal dissipation associated with the inefficiency.

From the standpoint of (a) inefficiency becomes significant during near-Mars operation when array power is limited and during any phase of battery operation because of limited watt-hour capacity. Assuming the existence of an 8 percent near-Mars array margin with a generation of 400 watts, a 32-watt increase in the dissipation of a particular PCU could be tolerated without affecting system operation. Assuming a similar 32-watt fault during battery operation, about 64 watt-hours would be drained from the battery for the maximum battery usage period of about 2 hours. This would be well within the capacity requirements of the battery. Thus, an appropriate limit for an allowable decrease in efficiency would be about 20 to 30 watts.

Concerning the second criterion relative to possible damage to other spacecraft equipment, it is judged that the packaging techniques used for the typical PCU's considered herein

would permit the added 20 to 30 watts of dissipation. Specific analyses would be required to verify this.

The need for efficiency fault detection presupposes that such a fault could occur without the simultaneous occurrence of a voltage output fault. Indeed, as analyzed in Section 5.1.4.1.5. it does not appear likely that a 20- to 30-watt efficiency fault could be sustained very long without causing damage of a nature that would result in output voltage dev'ations. For this reason it does not appear necessary to consider the use of efficiency detectors, though the inherent ruggedness of certain circuit elements might overrule this general conclusion.

5.1.4.2.3 Time Limits

Transient performance deviations may occur as a result of step changes in load or the time to clear particular load faults. For these reasons it is necessary that indicated PCU faults exist over finite time periods that are larger than those associated with the above transient conditions before any PCU transfer action is taken.

Due to the many uncertainties associated with predicting the transient behavior resulting from step load changes or load fault clearing, it is evident that PCU fault transfer should be delayed as long as possible. At the other extreme, the upper limit of delay time is established by acceptable outage times which it is, of course,desirable to keep as short as possible.

For the Mariner class of power systems, it is estimated that voltage deviation transients resulting from step load changes may persist for as long as 25 milliseconds. Concerning load fault clearing, it is estimated that this can be accomplished within a period of 10 to 100 milliseconds as described in Section 5.1.5. Thus, transients not resulting from PCU failure are not expected to last longer than 100 milliseconds.

As a measure of safety, it appears appropriate to increase the fault sensor delay time by a magnitude to a length of one to two seconds.

5.1.4.3 Efficiency Sensor Analysis

As mentioned in the previous section, it does not appear necessary to consider the use of PCU efficiency detectors since it is probable that PCU failure would be manifested through voltage measurements which employ less complex detectors. To support this conclusion, the behavior of the MM '69 boost regulator rated at 250 watts and a nominal efficiency of 90 percent was examined considering a variety of failures that would appear as a loss of efficiency.

The approach taken was to assume the existence of additional thermal dissipation within each of the major power components of the boost regulator, specifically the power transistors, capacitors, transformers and chokes. The added thermal dissipation would result from a failure of the component and would appear as an overall decrease in PCU efficiency.

Using appropriate form factors for each component, and assuming mounting on a heat sink operating normally at 75°C, thermal analyses were conducted to predict the temperature of the critical region of each component as a function of thermal dissipation. Component failure was presumed to exist when the temperature reached a maximum allowable level based on manufacturer's data. Since average temperatures were predicted in these analyses, the presumed failure appears to be a safe assumption since any actual failure hot-spot temperature would be appreciably higher.

Figure 5.1.4-6 summarizes the results of these analyses and shows the additional power loss or thermal dissipation for each component at which failure is predicted. Except for the class T transformer, failure is generally predicted well below an efficiency decrease of 20 watts. It is also presumed that under the elevated temperature conditions, the component failure would be sufficiently severe as to cause an overall regulator malfunction that would be manifested as an output voltage deviation. For this reason and the fact that an efficiency decrease of 10 to 20 watts is insufficient cause for fault transfer (see previous section), the need for efficiency sensing does not appear warranted.

The detailed analyses for the component parts considered are presented in the following paragraphs.

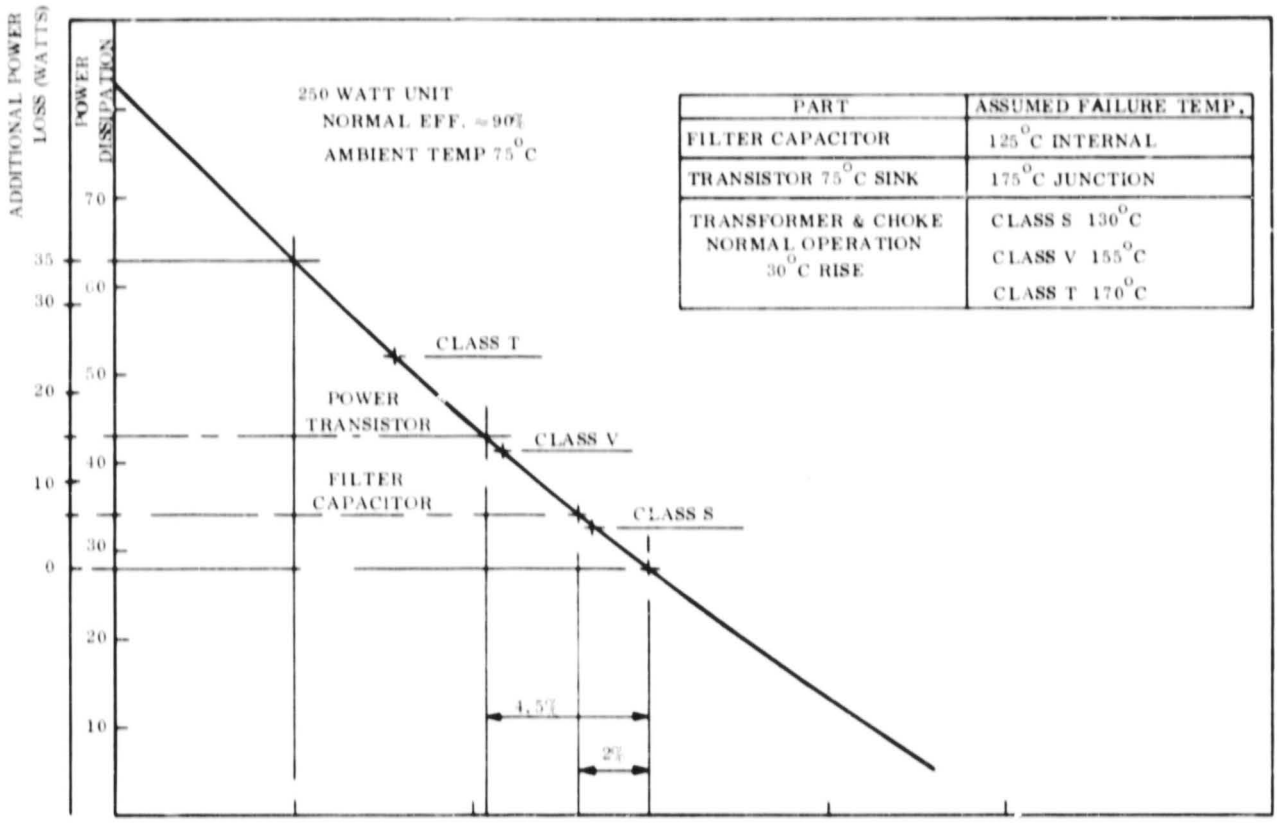


Figure 5.1.4-6. PWM Regulator - Efficiency Summary (Steady State)

5.1.4.3.1 Capacitors

Representative capacitors most commonly used in PCU input and output filters are similar to Sprague 310D and GE350D(29F) types. The failure considered conservatively distributes the heat evenly in the capacitor even though it is recognized that the probable failure is a local fault causing local heating.

The parameter of the capacitor which normally distributes heat evenly throughout the capacitor is the equivalent series resistance (ESR). The power dissipation may be determined in terms of the ESR as a function of heat sink temperature, frequency, and capacitor case size. General Electric design data for electrolytic capacitors (application information 121EC) was used in considering two types of capacitors: (a) a single tubular capacitor in a D3 case size; (b) multiple tubular capacitors in a rectangular KSR10 case size. Table 5.1.4-3 defines the power dissipation capability based on the 121EC application information. The capacitor can dissipate approximately 6 watts on a heat sink of 75°C at

Table 5.1.4-3. Efficiency Sensor Requirements-Capacitor Thermal Dissipation

Method No. 1

		Curves	Table	D3	KSR 10
(1)	ESR - At 75°C	15	16	0.22 ohm	0.072 ohm
(2)	Permissible RMS voltage @ 4000 Hz	21, 22, 23	--	2.1 volts	1.57 volts
(3)	X_c	1	--	1.5 ohm	0.17 ohm
(4)	Permissible RMS current $\frac{V_{RMS}}{X_c}$	Calculated		1.4 amps	8.8 amps
(5)	$P_D = (I_{RMS}^2)$ (ESR)	Calculated		0.39 watt	5.3 watts

Dimensions:

D3 - 1.44" x 0.375" DIA.
KSR 10 - 2.5" x 0.75" x 1.31"

Method No. 2 -- General check for Method No. 1

		D3	KSR 10
(1)	Area of Case - calculated	1.7 in^2	12 in^2
(2)	Watts Diss. per square inch (refer to Figure 5.1.4-7)	0.19 -0.43	0.19 -0.43
(3)	P_D - 75°C Ambient (Watts)	0.29 -0.73	2.3 - 5.3

NOTE - Curves and tables are from GE design data 121EC.

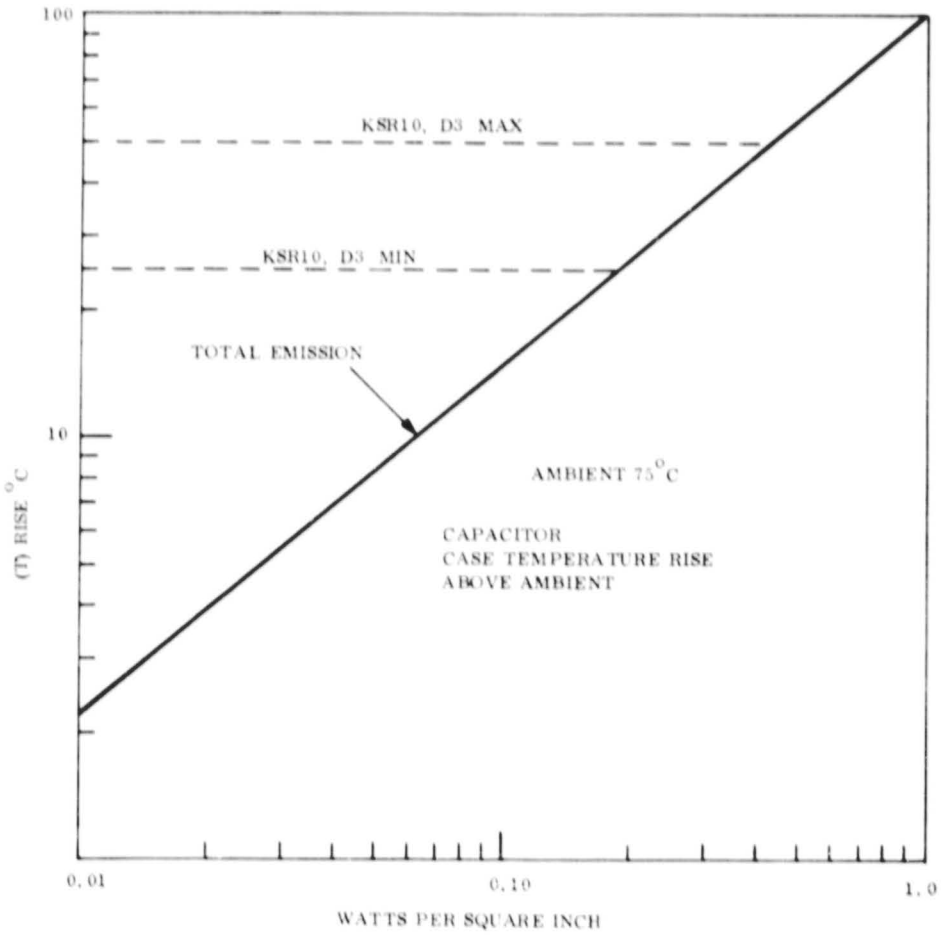


Figure 5.1.4-7. Capacitor Case Temperature Rise Above Ambient

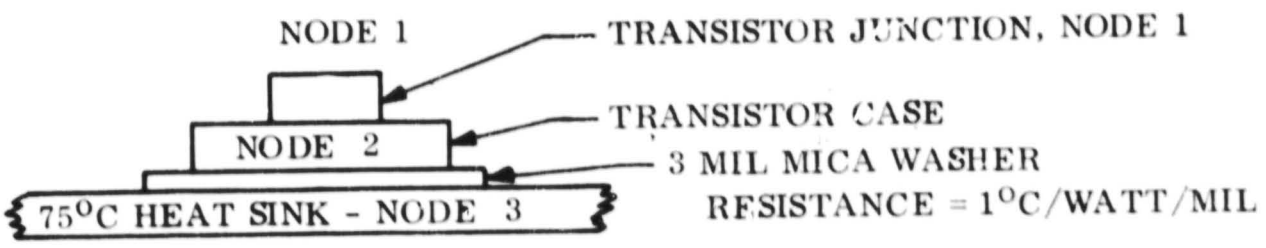
which time the maximum internal temperature would reach 125°C. An internal temperature of 125°C would result in rapid failure of the part.

5.1.4.3.2 Transistor

Representative transistors used in PCU's are fast switching transistors similar to Solitron SDT 8801 and MHT 8071. The thermal capacity for this transistor type is C_T = 0.34 watt-seconds/o_C relative to the total transistor assembly, and C_T = 0.015 watt-seconds/o_C relative to the transistor chip only. The failure considered is due to additional heat dissipation in the transistor. Since the thermal capacity of the chip is less than the total transistor assembly, the transistor chip will obviously reach the higher temperature before the transistor case. This analysis was performed to determine the maximum power dissipation of a transistor and the transient response as a function of time for various powers.

The transistor is considered to have failed when the junction temperature reaches 175°C.

A three node thermal model given in the sketch below was employed.



It consists of the junction (node 1), the transistor case node 2, a 3 mil mica washer and a 75°C heat sink (node 3). The thermal network parameters are as follows:

Node	Capacitance
1 (Junction)	0.015 watt-sec/°C
2 (Transistor Case)	0.34 watt-sec/°C

Nodes	Thermal Resistance
1-2	1°C/watt
2-3	3°C/watt (Case 1)
	6°C/watt (Case 2)

It is noted that a range of thermal resistance (from 3 to 6°C/watt) was studied to encompass possible effects of contact resistance at the surfaces of the mica washer, etc. The range for the total thermal resistance between the junction and the heat sink is therefore 4 to 7°C/watt. The results of the analysis is given in Figure 5.1.4-8 where junction temperature is plotted as a function of time for various power dissipations. The shaded regions depict the domain for the range of thermal resistances (4-7°C/watt) between the junction and the 75°C heat sink. (The shaded region was omitted for the 20-watt power dissipation since

this overlapped the 30-watt power condition.) In all cases the equilibrium temperatures are reached very quickly (less than 10 seconds) as would be expected because of the very small thermal capacity of the junction. Figure 5.1.4-9 is a cross plot of Figure 5.1.4-8 showing the equilibrium temperatures as a function of power dissipation for the two thermal resistance values of 4 and 7°C/watt between the junction and heat sink. The limiting junction temperature of 175°C is reached for power dissipations somewhere between approximately 14 and 25 watts for the encompassing range of thermal resistances considered.

5.1.4.3.3 Transformers and Chokes

Suitable transformers and chokes for PCU's are those satisfying the requirements of MIL-T-27. Transformer failure is based on the maximum temperature rating of transformer materials -- the limiting item is usually the magnet wire.

The transformer classes considered are:

S - 130°C,

V - 155°C,

T - 170°C, and

U > 170°C (Max temp specified)

The construction and usage determines the selection of materials, and hence, defines the transformer class. Table 5.1.4-4, Part I defines the basic assumptions for the magnetic part, and Part II defines the failures where 13 watts represents an efficiency change from 96 to 94 percent and 33 watts represents an efficiency change from 96 to 86 percent. Steady state temperature rise and temperature are tabulated.

Since the time constant of the transformer under this ideal failure is considered to be long in comparison with transistors and capacitors, a transient analysis was performed to establish the time to reach the temperatures defined in Table 5.1.4-4.

Table 5.1.4-4. Transformer-Choke Steady State Temperature Data

PART I				PART II		
NORMAL MODE (200 WATT UNIT)				FAILURE MODE[5]		
Design Efficiency	Temp Rise °C	Power Dissipation (1) Watts	Thermal Resistance °C/Watt	Temp Rise (2) / Temp	Temp Rise (3) / Temp	Temp Rise (4) / Temp
0.96	10	8.5	1.175	15.3 / 90.3	25.9 / 100.9	38.8 / 113.8
0.96	20	8.5	2.35	30.5 / 105.5	51.7 / 126.7	77.5 / 152.5
0.96	30	8.5	3.53	45.9 / 120.9	75.6 / 150.6	116 / 191
0.96	40	8.5	4.70	61.1 / 136.1	103 / 178	155 / 230
0.96	60	8.5	7.05	91.7 / 156.7	155 / 230	233 / 308

NOTES:
1. 8.5 Watts 0.96 Eff
2. 13 Watts 0.94 Eff
3. 22 Watts 0.90 Eff
4. 33 Watts 0.86 Eff
5. Heat Sink Temp 75°C

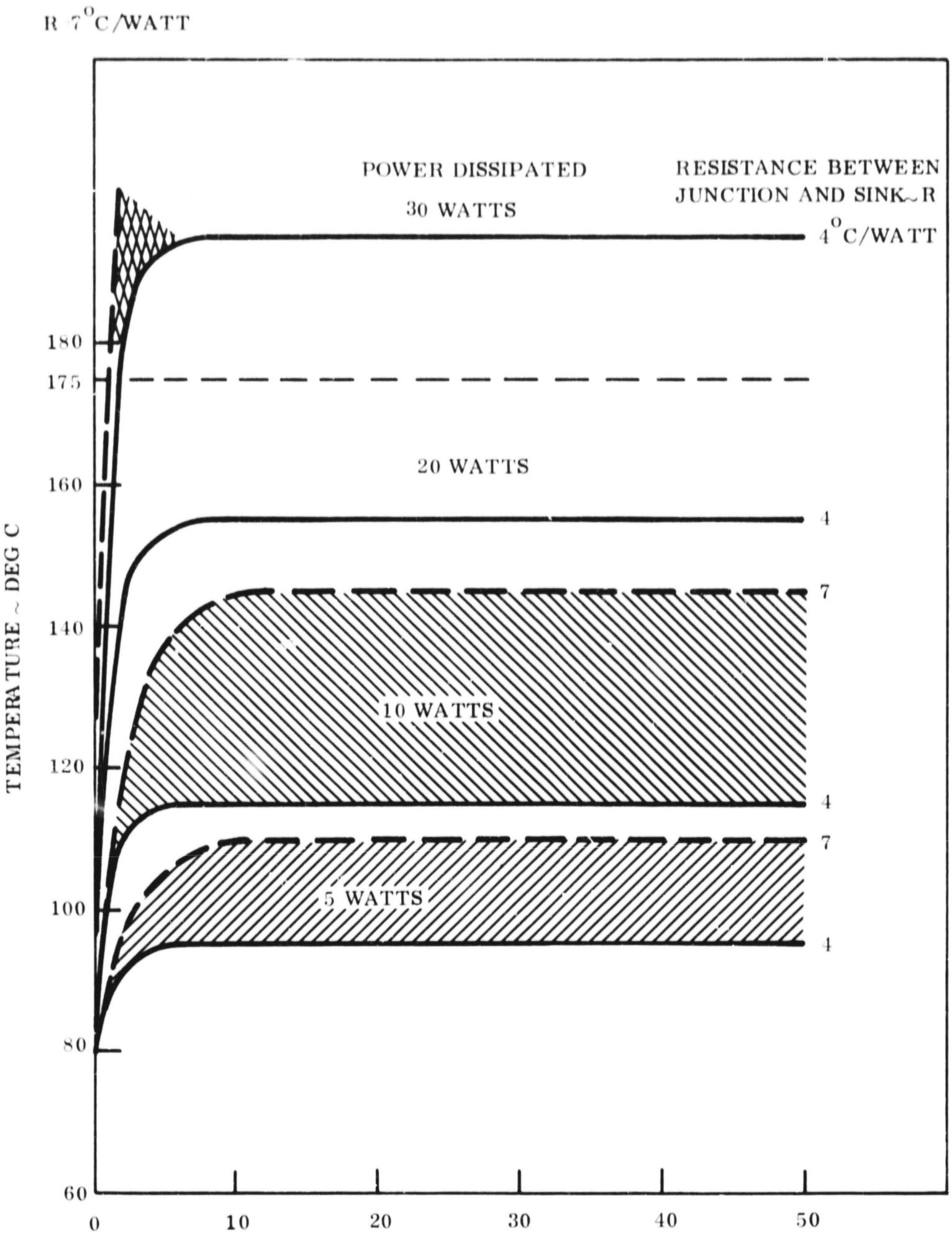


Figure 5.1.4-8. Transistor Junction Temperatures With a 75° Heat Sink

TRANSISTOR JUNCTION EQUILIBRIUM TEMPERATURES
WITH A 75°C HEAT SINK

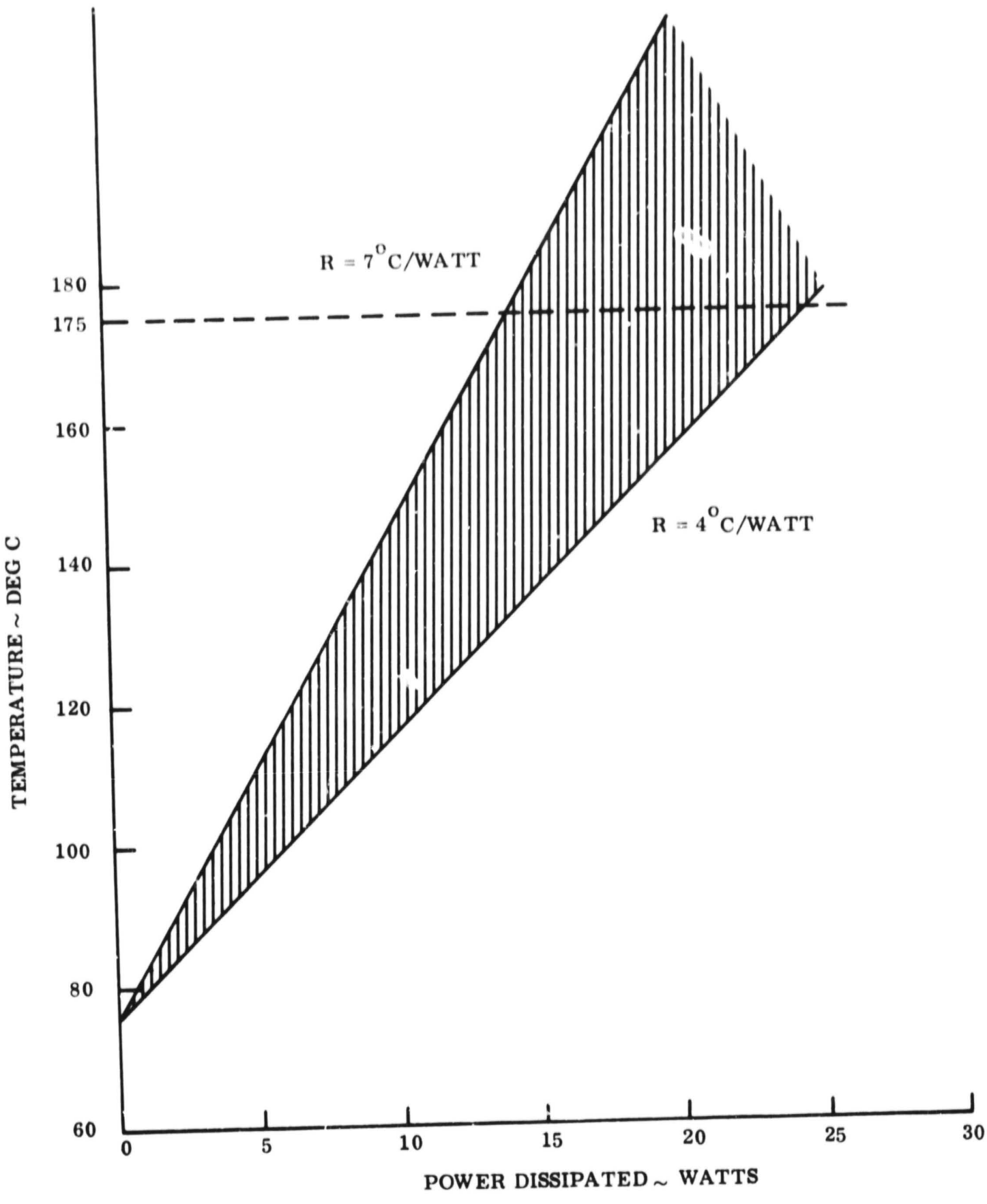


Figure 5.1.4-9. Transistor Junction Equilibrium Temperatures with a 75° Heat Sink

The transformer mass is composed of 25 percent iron, 50 percent copper and 25 percent potting compound. An average specific heat of 0.16 $\frac{\text{Btu}}{\text{lb}\ ^{\circ}\text{F}}$ was calculated for the two pound transformer.

It can be shown that for a lumped mass of thermal capacitance C, at an initial temperature of T_0, dissipating power Q, and conductivity coupled with a thermal resistance of R to a heat sink at T_0, the time τ required to reach a temperature T is given by

$$\tau = -RC \ln \left(1 - \frac{T-T_0}{QR} \right)$$

This equation was used to determine the transient temperature histories for the aforementioned range of design efficiencies (dissipated power) and thermal resistances. Representative results are given in Figure 5.1.4-10 showing data for one value of the thermal resistance with power as a parameter. In each case the final temperature indicated on the curve is within approximately 1°F of equilibrium temperature. Because of the relatively high thermal inertia of the transformer, it takes anywhere from 2600 seconds and 20,000 seconds to reach equilibrium; the higher the resistance the longer it takes to reach equilibrium and, of course, the higher is this steady-state temperature. The temperature limits for transformer classifications "S", "V" and "T" are noted on the ordinate scales. Figure 5.1.4-11 shows the equilibrium temperature as a function of power with thermal resistance as a parameter.

5.1.5 LOAD FAULT PROTECTION

Protection of the power system against load faults is possible through the use of fuses or circuit breakers. Figure 5.1.5-1 shows a comparison of fuse and circuit breaker characteristics. Circuit breakers have a relatively constant time response above certain loads while the fuse response time decreases with increasing load.

The Heinemann circuit breaker is a 400 Hz, manually resettable, flight qualified, 0.05 to 20-ampere breaker. An electrically resettable type is presently being developed. The Teledyne circuit breaker is a direct current, magnetic latching, 0.01 to 0.15 ampere current sensitive

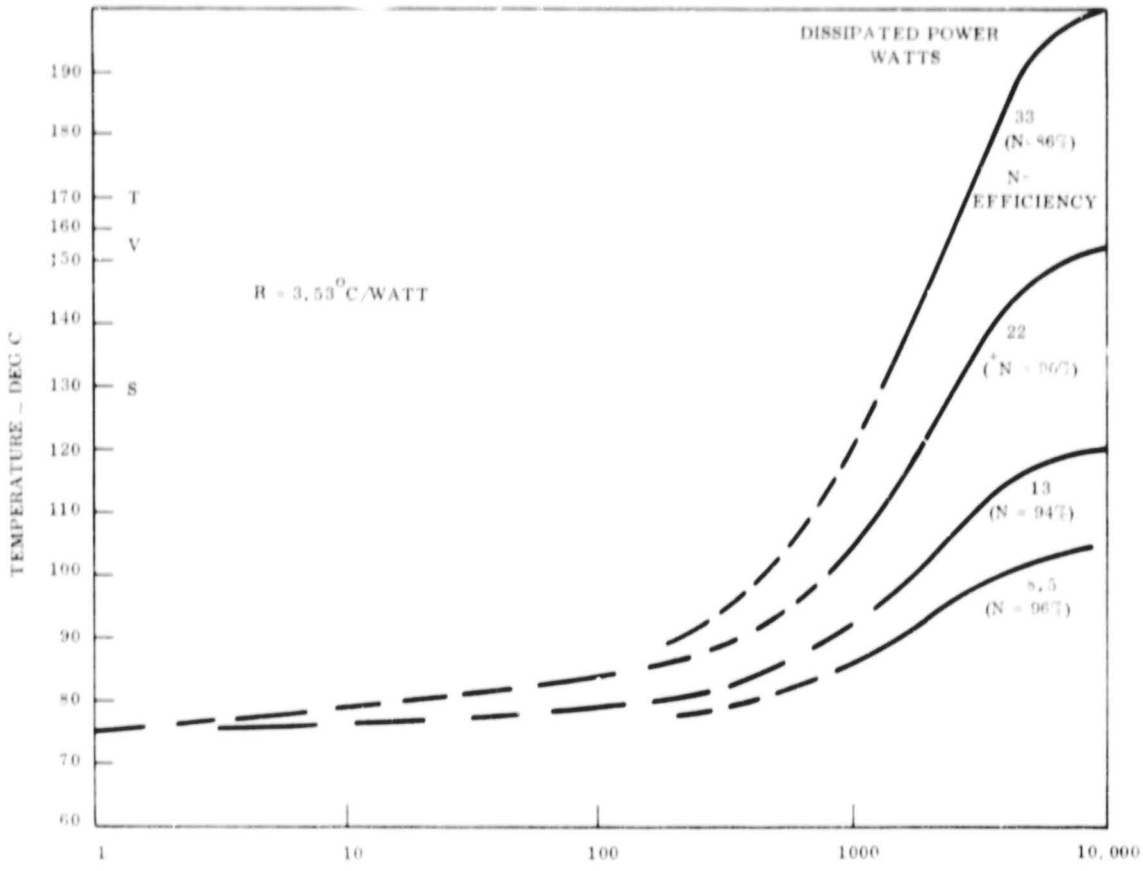


Figure 5.1.4-10. Temperature Rise of 200 Watt Transformer Coupled With a 75° Heat Sink

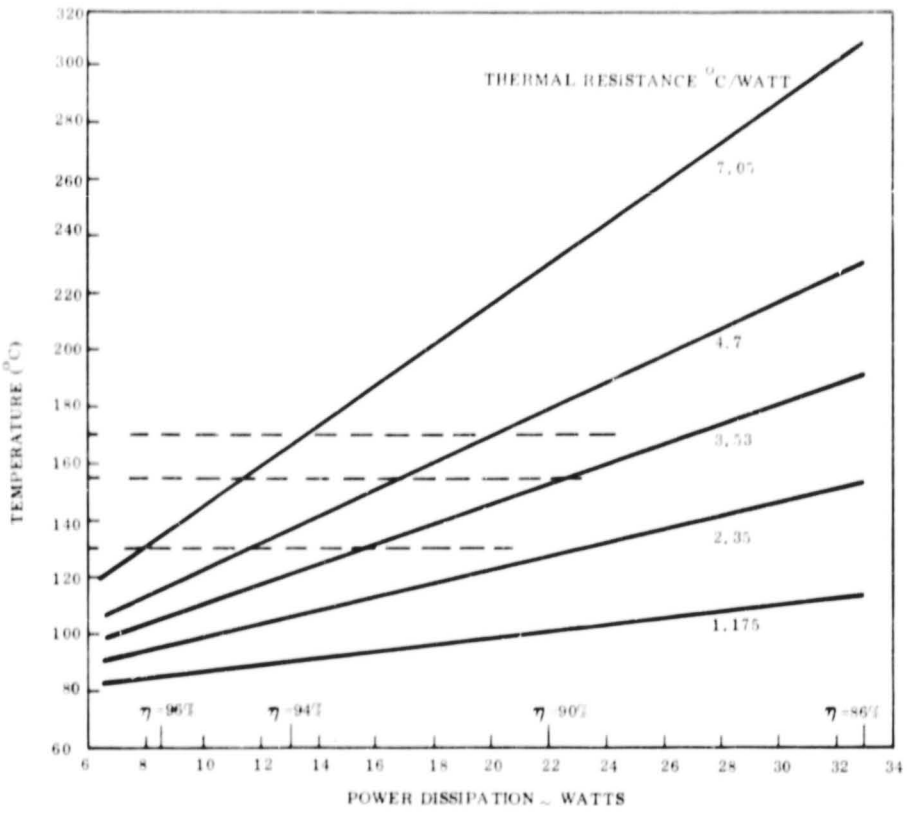


Figure 5.1.4-11. Transformer Equilibrium Temperatures Versus Power Dissipation

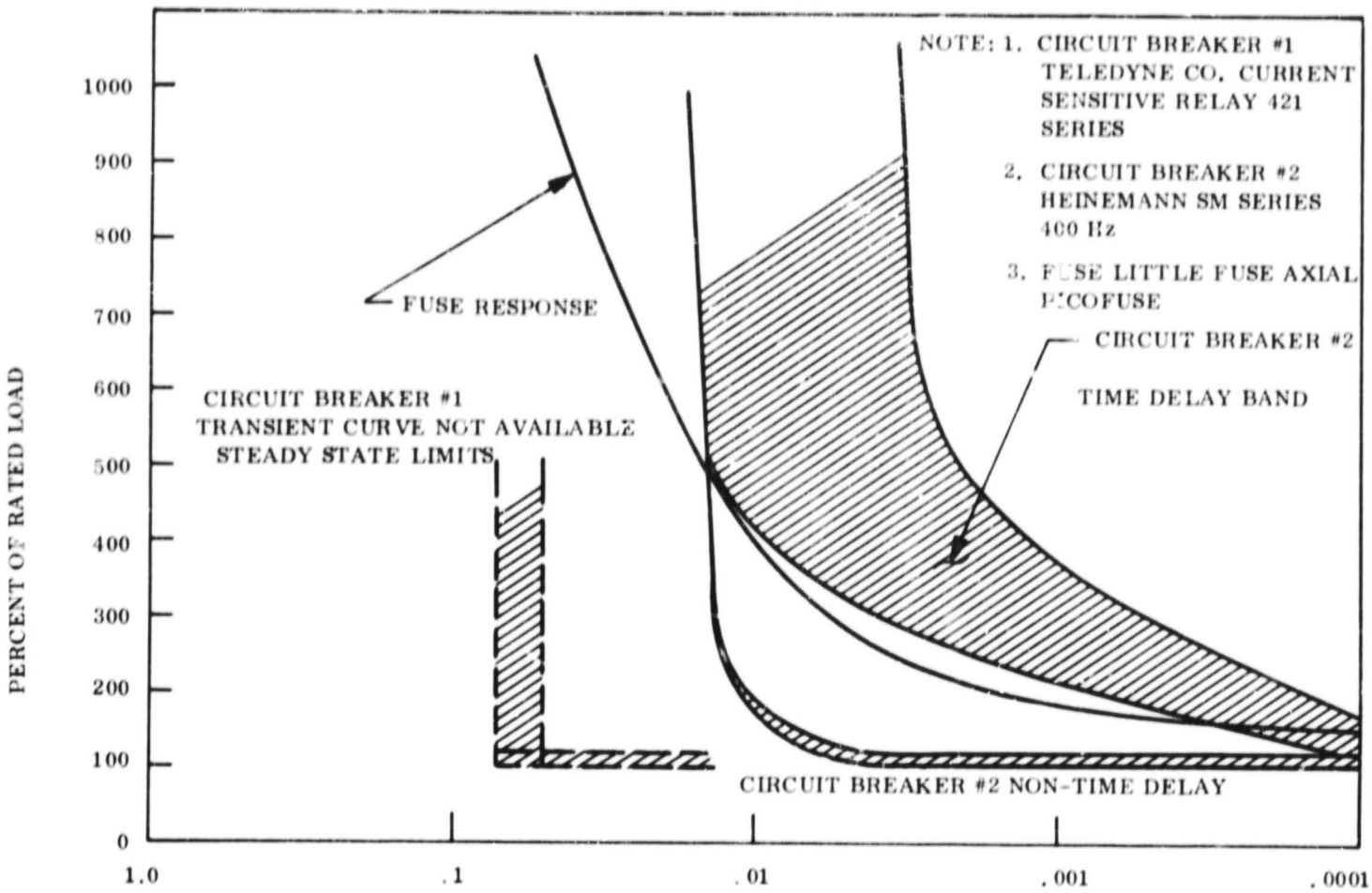
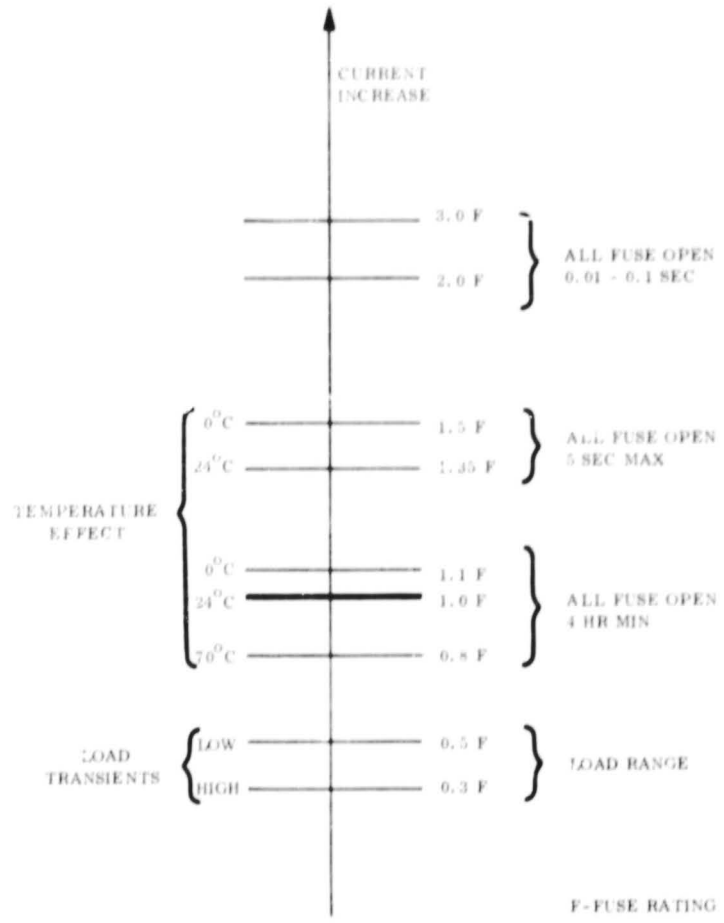


Figure 5.1.5-1. Fuse-Circuit Breaker Comparison

relay that is electrically resettable. The Littlefuse fuse is a subminiature axial picofuse available in current sizes from 0.125 to 5.0 ampere and is presently used on the Nimbus spacecraft.

All further discussion pertains to fuses since they are more generally available and proven.

According to certain information, the criterion for the nominal rating of a fuse pertains to that current which will cause the fuse to open in not less than 4 hours and will cause it to open in less than 5 seconds with an applied current of 1.35 times its rating. It is usual practice to verify this performance at an ambient temperature of $24^{o}C$. Using this criterion, more general fuse behavior is summarized on Figure 5.1.5-2 for a nominal fuse rating of F (in amperes). It is general practice to select a fuse having a rating of 2 to 3 times the load rating for proper margin allowance and to assure that the fuse will not open during normal operation.



DATA SOURCE: LITTLE FUSE, FUSE TYPE AXIAL PICO FUSE

Figure 5.1.5-2. Load/Fuse Sizing Chart

From the fuse response curve shown on Figure 5.1.5-3, the current required to open the fuse in a specified time may be estimated. To assure a full open in 0.1 seconds, the curve indicates the current must be from about 1.5 to 2.5 times higher than the fuse rated value taking the fuse uncertainty characteristics into account. Since the fuse is selected to have a rating 2 to 3 times larger than the load being protected, this implies that in the most extreme case, the current to open the fuse would have to be 7.5 times larger than the normal load current.

These characteristics have a direct bearing on PCU design requirements, or given a particular PCU, they define the maximum load that can be safely fuse-protected with that PCU. To illustrate, assume a 200-watt PCU is used which can tolerate an overload of 150 percent for 0.1 second at rated voltage without incurring self damage. The PCU supplies multiple fused loads, and it is desired to determine the maximum size of any individual load.

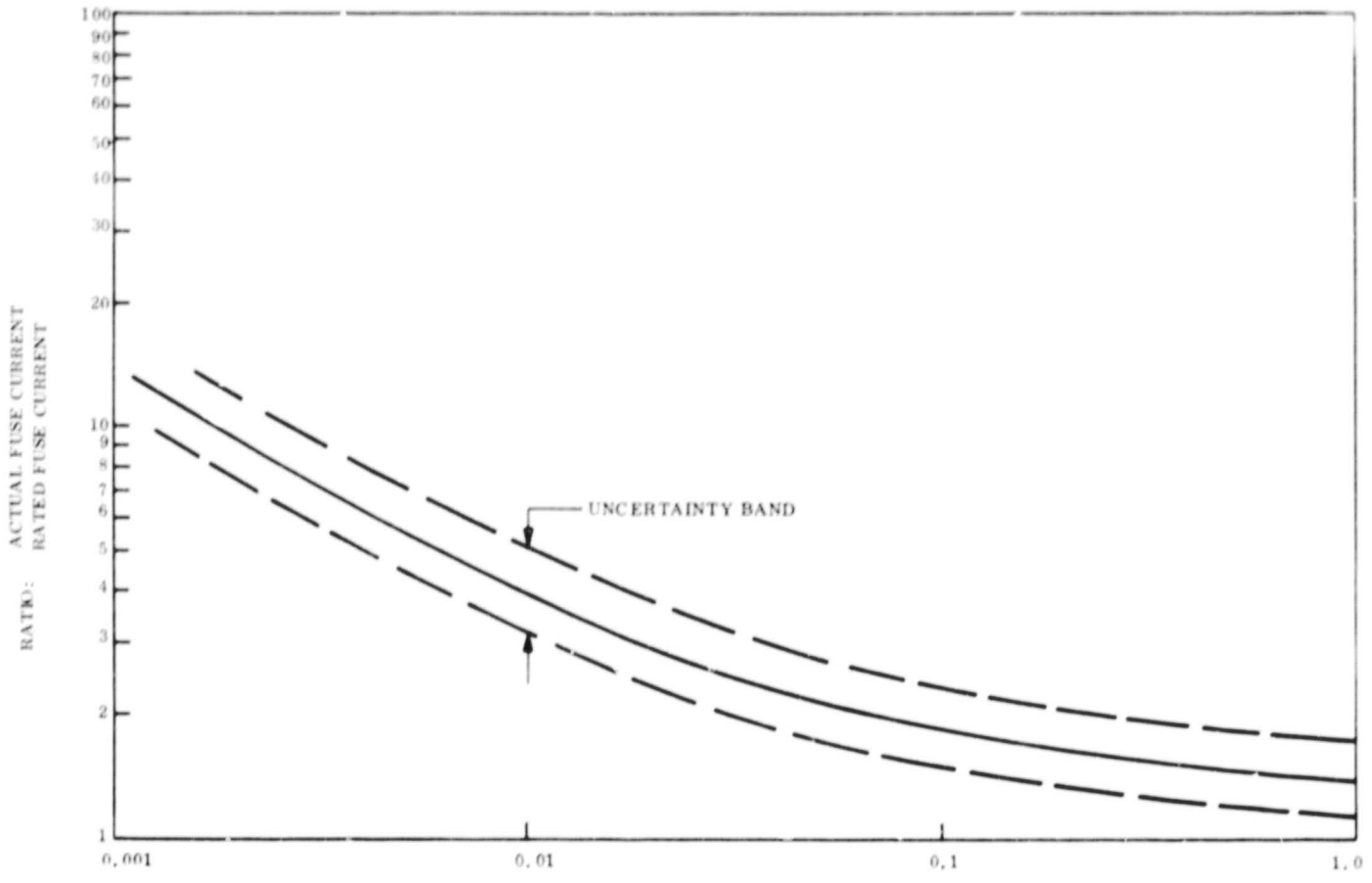


Figure 5.1.5-3. Typical Fuse Time Response Characteristics

Assuming operation at full load, the PCU has a 100-watt overload capability for 0.1 seconds. As stated previously, about 7.5 times the normal load current is required to open a fuse associated with a faulty load. Thus, discounting the normal load current itself, the 100 watts can be devoted to 6.5 times the load current, or at normal voltage, the equivalent of a 15.5 watt load.

In order to prevent damage to the PCU, it is important then that fused loads be limited in accordance with these considerations.

The PCU characteristics assumed in the fuse sizing discussion above are limited to a specific level of load impedance. With increased load (lower impedance), the PCU would ultimately be destroyed. Fuse sizes were specifically limited with this in mind. It is

possible to incorporate circuit techniques that limit the PCU current permitting operation into low load impedances though at a sacrifice of output voltage requirements. Such performance characteristic modifications could be useful for PCU self-protection and at the same time, could enhance fault clearing capability. Figure 5.1.5-4 illustrates the nature of such possible modifications. Curve A designates an unmodified PCU indicating the impedance level that would result in failure. Curve B represents a current limiting modification permitting operation into low impedances. At the load fault impedance shown, sufficient current would be available to clear the fuse associated with the faulty load over longer periods of time since the internal PCU power dissipation is reduced.

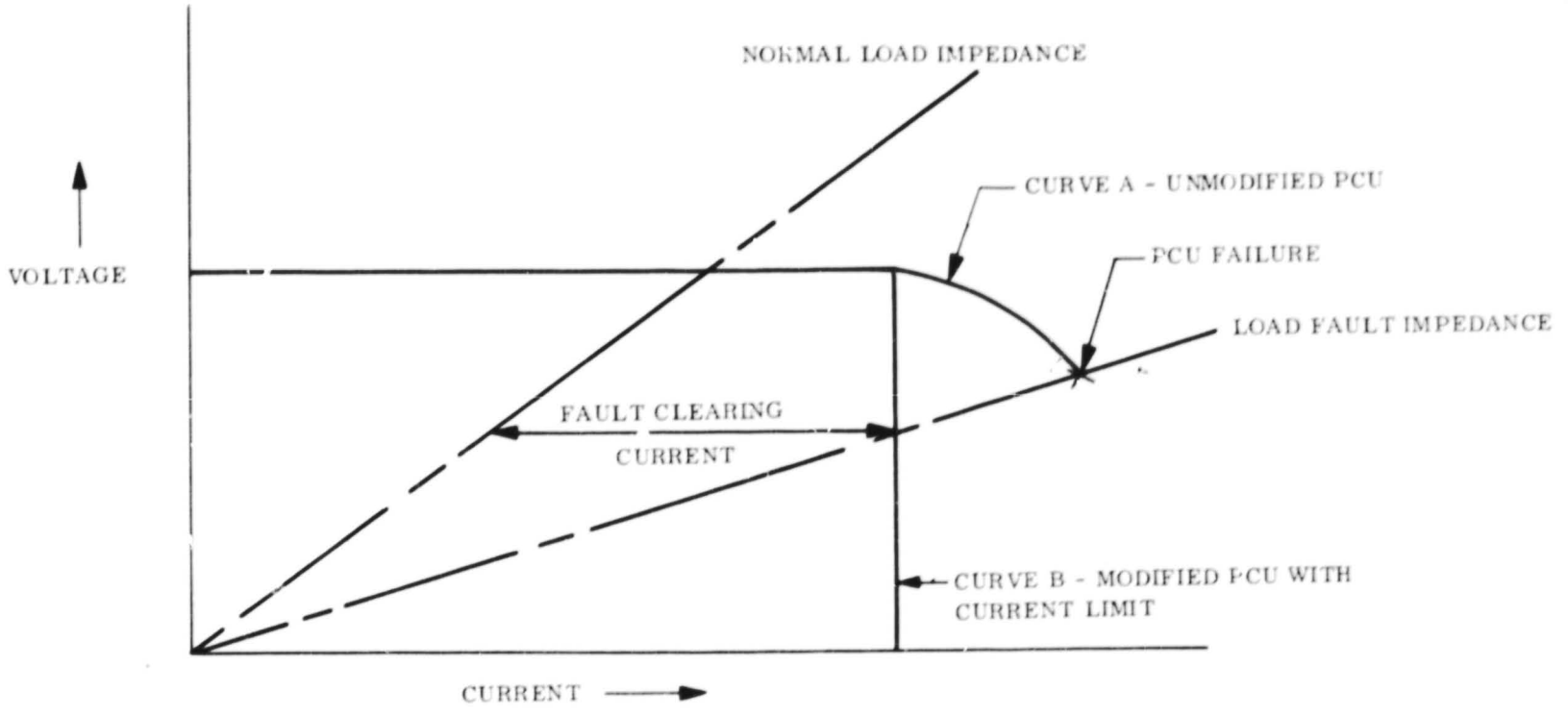


Figure 5.1.5-4. PCU Load Fault Protection

5.1.6 SHUNT SYSTEM TRANSIENT RESPONSE

The transient response of the power system to step load changes on the 2.4 kHz distributed voltage are reflected directly through the inverter to the regulated bus, since the inverter has no output filter and the equivalent series inductance presented by the power transformer

and input filter is small. Therefore, the transient response need only be discussed with reference to the regulated bus.

The regulated bus is provided by two regulators--shunt regulator and boost regulator. During the operation of either regulator, the output capacitor of the boost regulator provides energy ballast for increasing or decreasing loads. The response of the shunt regulator to load and source changes is considerably faster than the response of a switching type regulator because it does not require output filtering. Thus, transient effects result principally from boost regulator operation. The parallel connection of the shunt regulator and boost regulator provides an improvement in decreasing load transient response primarily due to the voltage limiting of the shunt regulator. During battery operation and abruptly increasing loads only, the transient response of the boost regulator determines the transient overvoltage characteristic. This response, however, is expected to be well below 50 milliseconds for a 20 percent load change such that the failure detector timing requirements are satisfied. Factors which influence the response of the boost regulator are discussed in the following paragraphs along with suggestions for improvement.

Transient response of the boost regulator to step load changes is a function of energy storage of the output capacitor, equivalent series inductance, and control loop characteristics. Figure 5.1.6-1 is an equivalent circuit for a typical switching type regulator. The desirable features for step load changes are to have a large output capacitor for high energy storage, to have low series inductance so that the source could supply some of the load change, and to have a high frequency response control loop so that the regulator characteristics correct for transient voltage deviations.

These desirable features have related effects. For example, the filter size is determined by the operating frequency, transformer turns ratio, ratio of switch on-time to total time of period, and the load. Usually the load (output ripple and modulation) has a greater effect on determining size than the operating frequency. Assuming that the load variations size

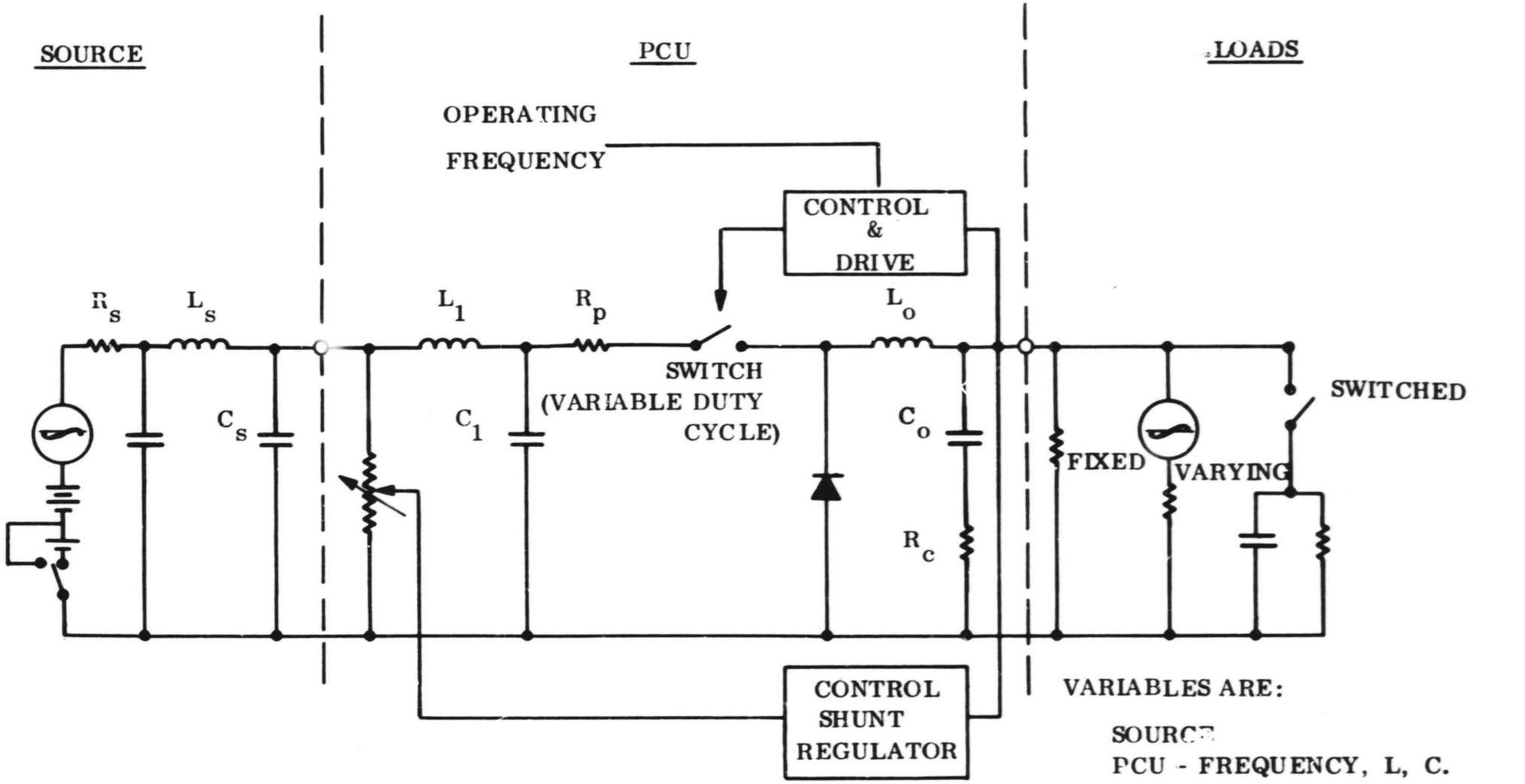
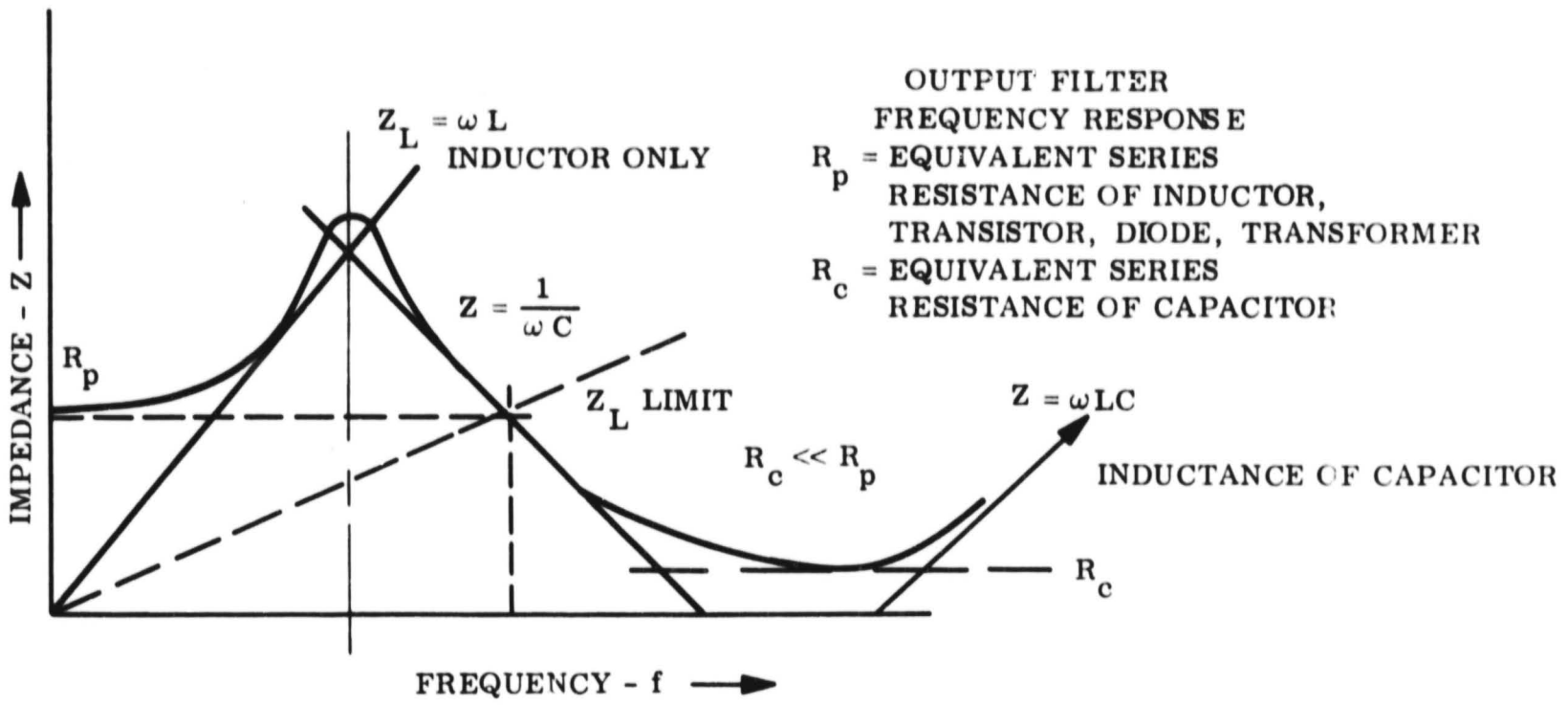


Figure 5.1.6-1. Transient Response Analysis Equivalent Circuit

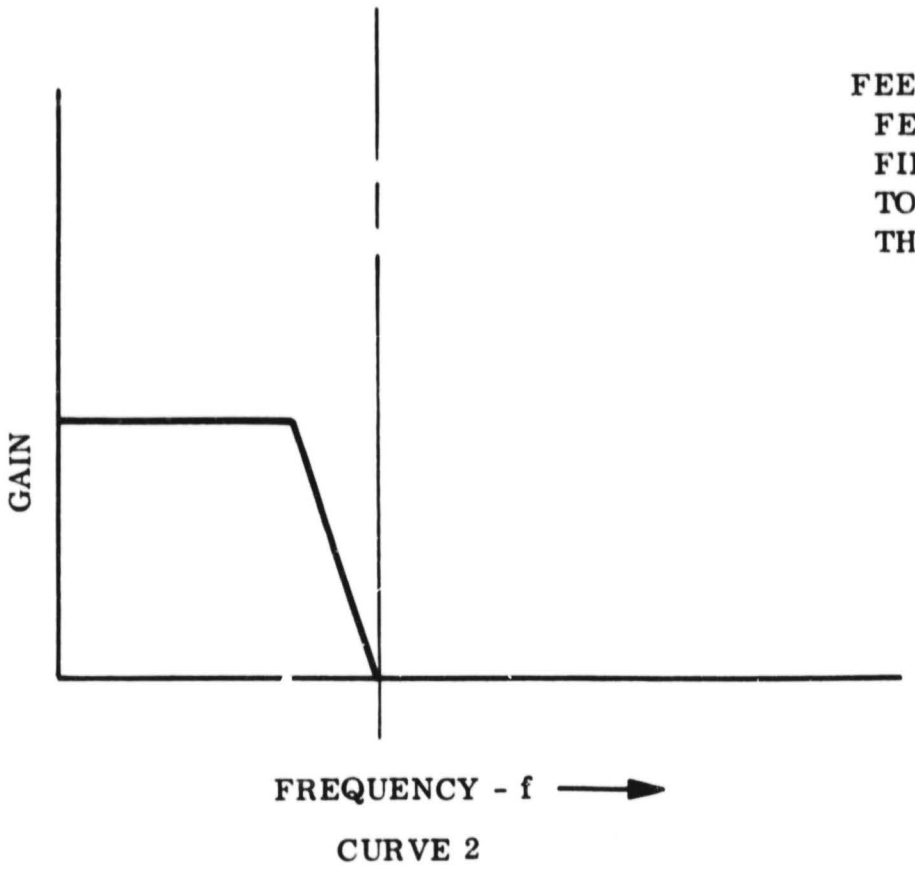
the output filter, then the filter most likely has a response which automatically forces the control loop to respond slowly; Figure 5.1.6-2 further explains this. Thus, transient response is a function of output filter impedance. If the control loop is not closed around the output filter, the output capacitor must be sized to present a low impedance to the dynamic load.

If the output capacitor were reasonably large, then the inductance of the LC output filter could be small to satisfy the load impedance. The inductor, L, is then primarily sized so that the switch does not look directly into the output capacitor causing excessive dissipation in the switch. On this basis, the inductor need only be sized to maintain a near constant current through the switch during the on-time of the switch. If the on-time of the switch were short, then the inductance could be reduced. Thus, an increase in switch driving frequency will reduce the inductance, L, and provide a faster response time to step load changes. Further, the response of the control loop is also shortened if the driving frequency is increased because the output filter response is at a higher frequency due to the lower inductance.



CURVE 1

OUTPUT FILTER
FREQUENCY RESPONSE
R_p = EQUIVALENT SERIES RESISTANCE OF INDUCTOR, TRANSISTOR, DIODE, TRANSFORMER
R_c = EQUIVALENT SERIES RESISTANCE OF CAPACITOR



CURVE 2

FEEDBACK CONTROL CHARACTERISTICS
FEEDBACK LOOP MUST CUT OFF BEFORE FILTER RESONANCE OR BE COMPENSATED TO PREVENT INSTABILITY BECAUSE OF THE 180^{o} PHASE SHIFT.

Figure 5.1.6-2. Output Filter Frequency Response and Feedback Control Characteristics

5.2 RELIABILITY STUDIES

5.2.1 INITIAL RELIABILITY SENSITIVITY STUDIES

5.2.1.1 Approach

It is very difficult to accurately predict or calculate the reliability of various piece parts, subunits of a blackbox or the complete blackbox, because of uncertainties in reliability data and shortcomings in reliability modeling associated with problem definition. Consequently, the approach taken on this study is to perform selected sensitivity studies in a parametric fashion to illuminate key questions concerning the operation of the subsystem elements.

Utilizing parametric sensitivity studies, we can plot results for specific points to be analyzed for the full range of reliability from 0 to 1, and then we can assess the relative importance of various questions, even though we do not know with any confidence the actual hardware reliabilities of the various elements. By way of illustrating this approach, and how the results of such studies can provide insight into certain fundamental questions, the first two examples, discussed separately in the following section, consider the cases of two series elements and two parallel elements. These examples, as well as the remainder of the analysis in this section, have been studied with the use of the remote access time sharing computer system.

5.2.1.2 Series Example

Figure 5.2.1-1 shows the block diagram being analyzed. R_π represents the reliability of one black box and R_N represents the reliability of the second black box. For the system to work both black boxes must work; hence, the series diagram. R_S is the reliability of the system and is:

$$R_s = R_\pi \times R_N \qquad (5.2.1\text{-}1)$$

Figure 5.2.1-2 is a plot of the system reliability, R_s, versus the reliability of the first black box, R_π. The parameter represents the reliability of the second black box, R_N.

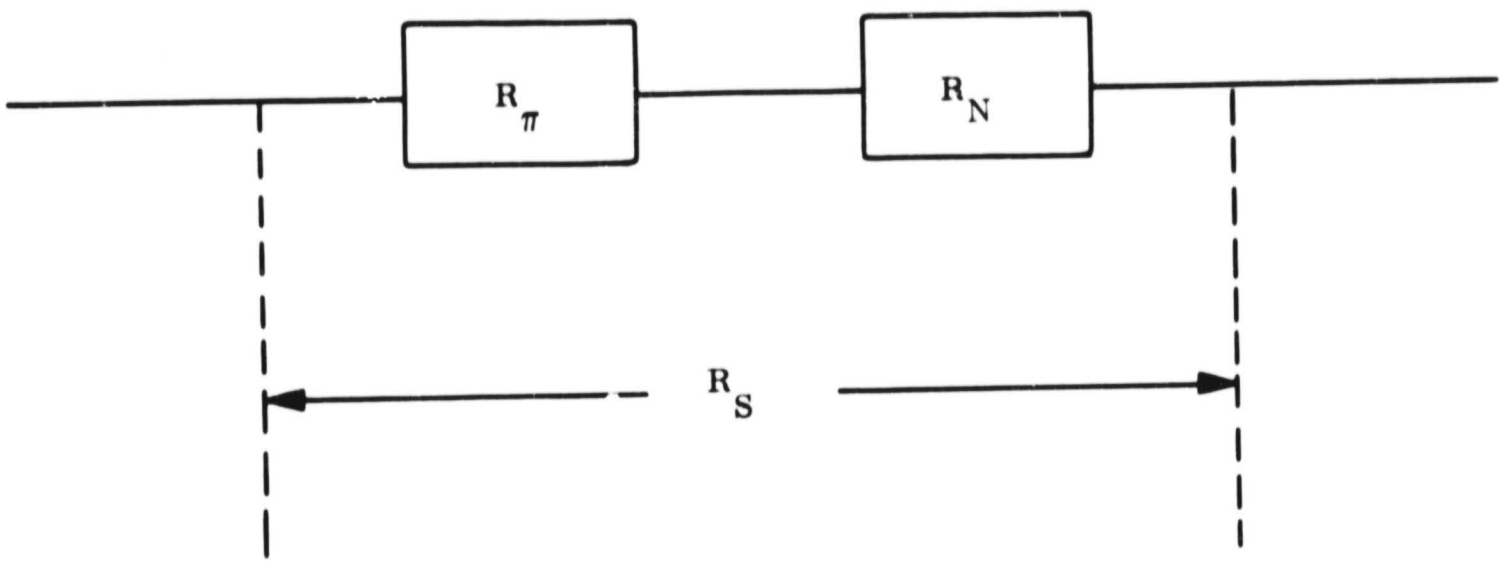


Figure 5.2.1-1. Series Block Diagram

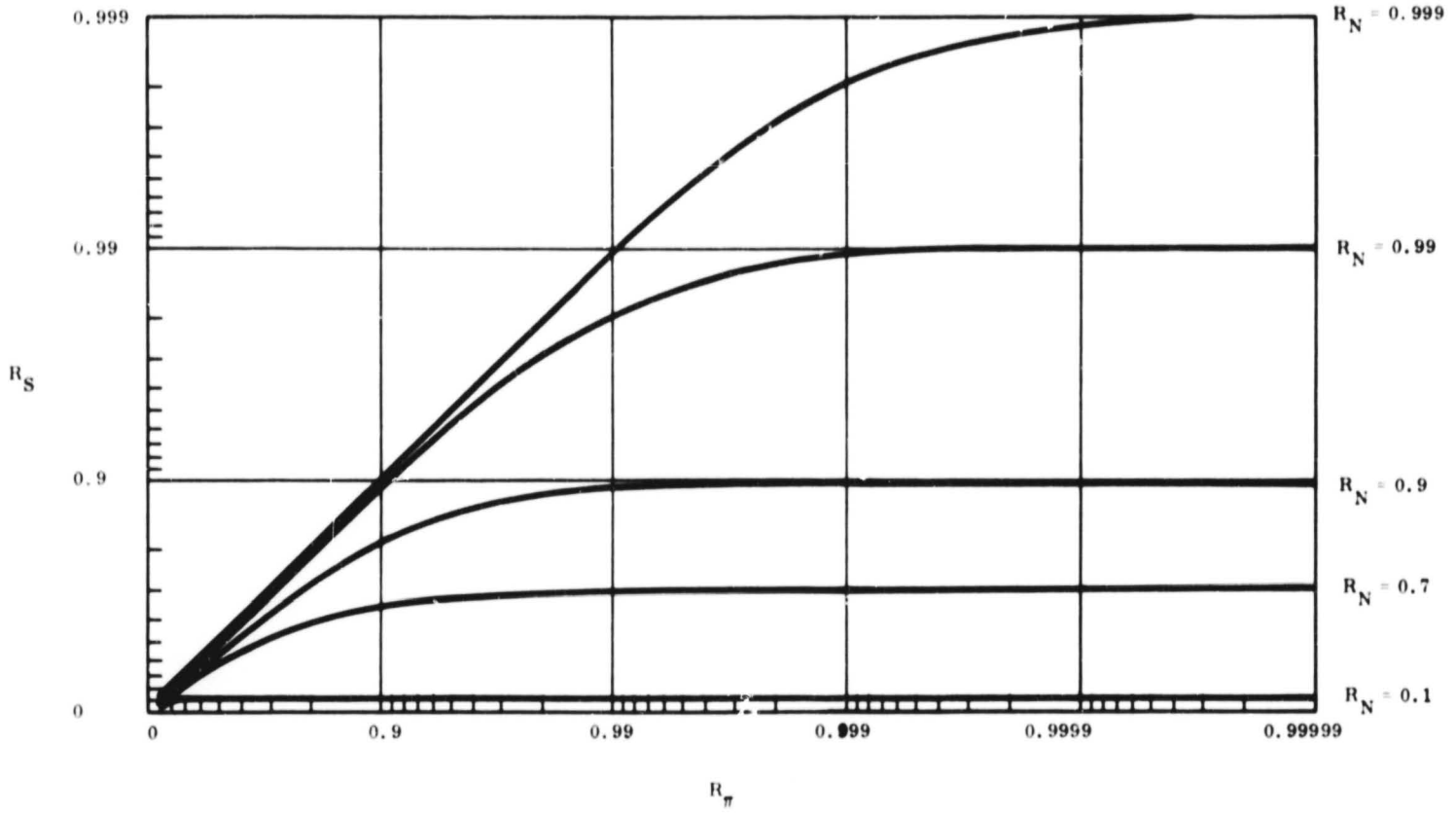


Figure 5.2.1-2. Series System Reliability

Conclusions

Several general conclusions concerning a series system can be seen from examination of Figure 5.2.1-2 and Equation 5.2.1-1.

a. R_π and R_N are interchangeable; consequently any statement made about one black box equally applies to the other.

b. The system reliability never exceeds the reliability of the lowest element.

c. The system reliability improves linearly with improvement of the lowest element until the lowest element is nearly as reliable as the highest element.

d. Once the most reliable element is about an order of magnitude better than the lowest element, no significant system improvement follows from further improvement of the highest element.

e. R_π and/or R_N can represent the reliability of a single black box or the reliability of several black boxes in series.

f. From b and c, above, it follows that to improve the system, effort should be concentrated on improving the least reliable element.

5.2.1.3 Parallel Example

Figure 5.2.1-3 shows the block diagram being analyzed. R_π represents the reliability of one black box and R_N represents the reliability of a second black box. The system works successfully if either black box works, hence the parallel diagram. R_s is the reliability of the system and is:

$$R_s = R_\pi + R_N - R_\pi R_N \qquad (5.2.1\text{-}2)$$

Figure 5.2.1-4 is a plot of the system reliability, R_s, versus the reliability of one black box, R_π. The parameter represents the reliability of the second black box, R_N.

Conclusions

Several general conclusions concerning a parallel system can be seen from Figure 5.2.1-4.

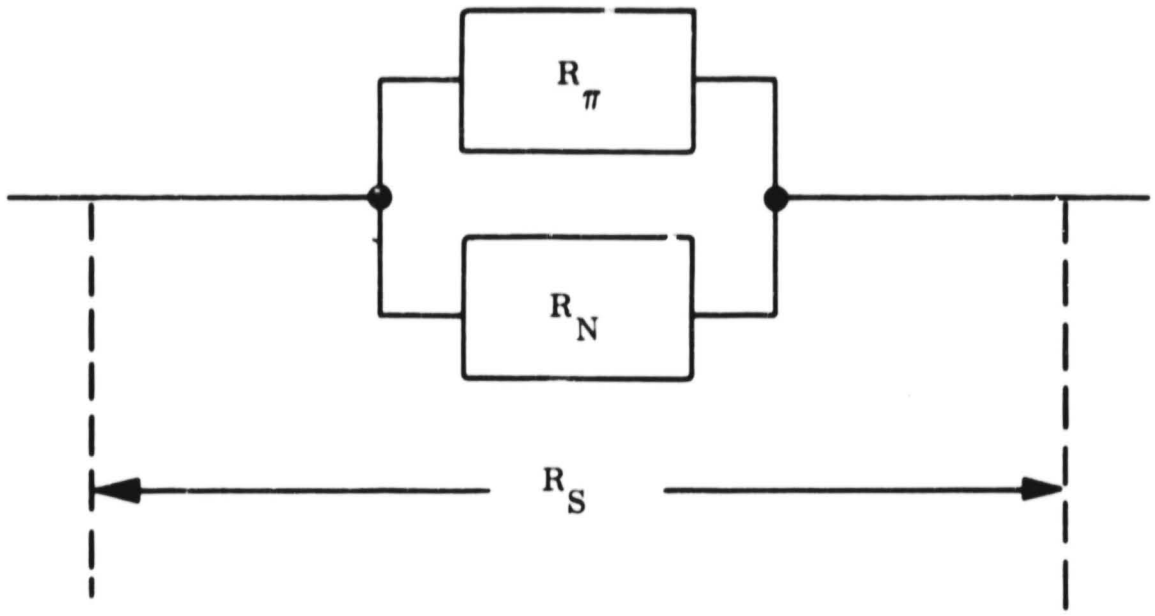


Figure 5.2.1-3. Parallel Block Diagram

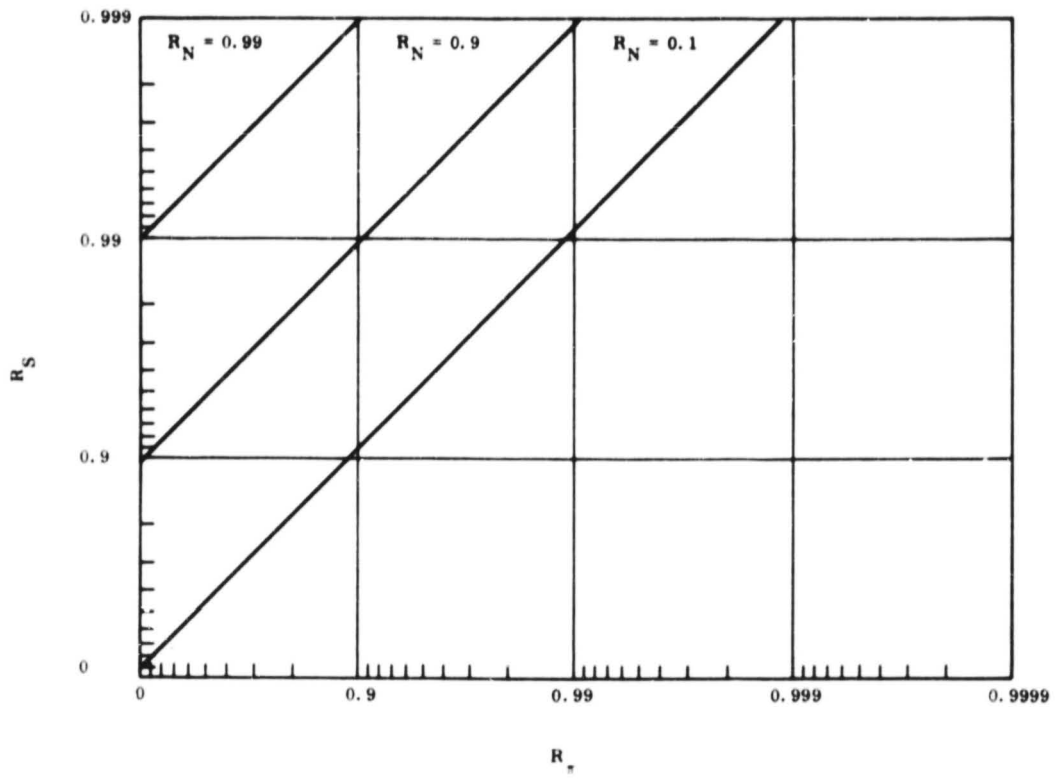


Figure 5.2.1-4. Parallel System Reliability

a. R_{π} and R_N are interchangeable, consequently any statement made about one black box equally applies to the other.

b. The system reliability always exceeds the reliability of the highest element.

c. The system reliability improves with improvement of either element.

d. The system reliability always improves with improvement of either element reliability: no matter what the relative reliabilities are.

e. R_{π} and/or R_N can represent the reliability of a single black box or the reliability of several black boxes in series.

f. From b, c, and d, it follows that to improve the system, effort can be applied to either element; hence, which element is easiest to improve would become the main criteria.

5.2.1.4 Fault Sensing and Switching

One of the major areas of interest on this study is the subject of switched redundancy for regulators and inverters. The use of a standby regulator and/or inverter in conjunction with a fault detection and switching system always raises the question of whether the system reliability might not have actually been degraded by the additional fault sensing complexity. The following sections describe studies aimed at illuminating this general question.

5.2.1.5 Cold Versus Hot Redundancy

Standby redundancy can be implemented in two ways:

a. Hot redundancy where the standby unit is always turned on

b. Cold redundancy where the standby unit is not turned on until the main unit has failed

Presumably cold redundancy would be the most reliable since the standby unit is not on until the main unit fails, hence, its operating life is shorter. The following analysis sheds some light on this specific question as well as the general subject of fault sensing and switching of a redundant element.

Figure 5.2.1-5, Part A, shows the basic circuit being analyzed, and Figure 5.2.1-5, Part B, the corresponding block diagram used to assess the system reliability.

R_R and R_I represent the reliabilities of the regulator and inverter, respectively. The A, B, and C blocks represent the reliability of the fault sensing and switching. The failure modes which are incorporated in the A, B, and C blocks are listed below:

A	B	C
Open top relay contacts	Pole of relays open	Open relay coil
		Welded top contacts
False detection and switching	Pole side relay connections open	Fault sensor fails to detect failure and/or switch over
		Bottom contact open

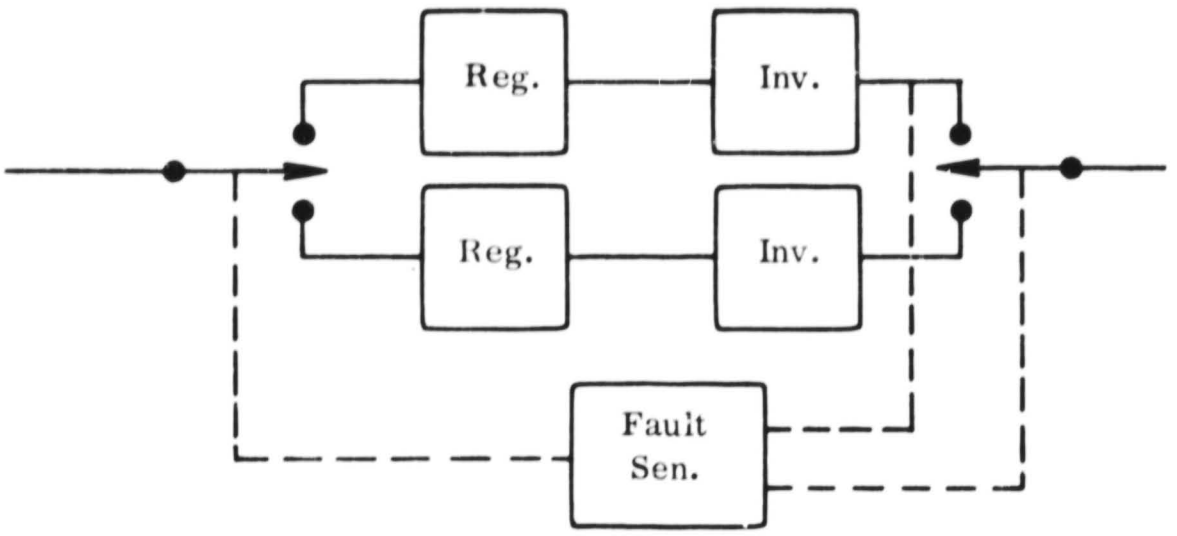
For the hot redundancy situation the total system reliability is:

$$R_s = [\, 1 - (1 - R_R\, R_I\, R_A)\,(1 - R_R\, R_I\, R_C)\,]\, R_B \qquad (5.2.1\text{-}3)$$

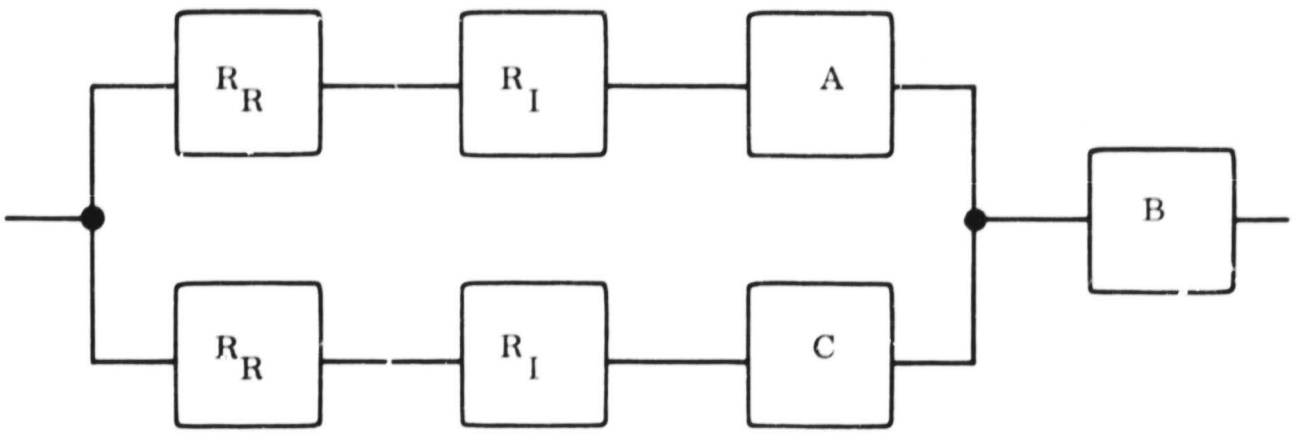
For the cold redundancy situation the total system reliability is:

$$R_s = e^{-(\alpha + \lambda_\beta)\, T} + \frac{\alpha}{\beta - \alpha} e^{-(\beta + \lambda_\beta)\, T} \left[e^{-(\alpha - \beta)\, T} - 1 \right] \qquad (5.2.1\text{-}4)^*$$

* This equation assumes: (1) the A block must work from the beginning of the mission until a switchover to the redundant string occurs, (2) the B block must work for the entire mission, and, (3) the C block must work from the time the standby chain is first used until the end of the mission. Actually most of the C block items must work only until a switchover to the standby chain occurs. This analysis was checked and the numerical results are essentially the same for either time of operation of the C block.



A



B

Figure 5.2.1-5. Paired Regulator Inverter

where:

$\alpha = \lambda_R + \lambda_I + \lambda_A$

$\beta = \lambda_R + \lambda_I + \lambda_C$

λ_i = the failure rate of the i^{th} component

T = mission time

all reliability functions are assumed to be exponential functions.

Conclusions

Figure 5.2.4-6, shows the system reliability, R_s, versus the "C" reliability, R_c, with "A" as a parameter, R_A. Figure 5.2.1-6, Part A, is for the case where we have poor black boxes whose reliabilities are $R_R = R_I = 0.9$. Figure 5.2.1-6, Part B, is for better boxes where $R_R = R_I = 0.99$. And Figure 5.2.1-6, Part C, is for very reliable black boxes where $R_R = R_I = 0.999$. The single string reliability for just the regulator and inverter is shown as a horizontal line in this illustration.

Since "B" is in series with the whole system, its reliability is very important to the problem (see Section 5.2.1-2) and must obviously be kept very high. For the following studies it is assumed perfect, hence, $R_B = 1.0$.

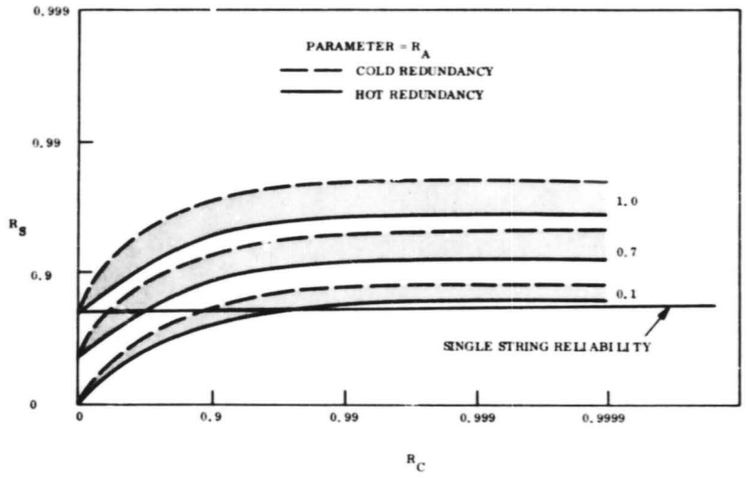
The following conclusions are drawn from Figure 5.2.1-6:

a. The redundant system is always more reliable than the single string system if the fault sensing reliability, R_A and R_C, is equal to or higher than the black box reliability, R_R and R_I.

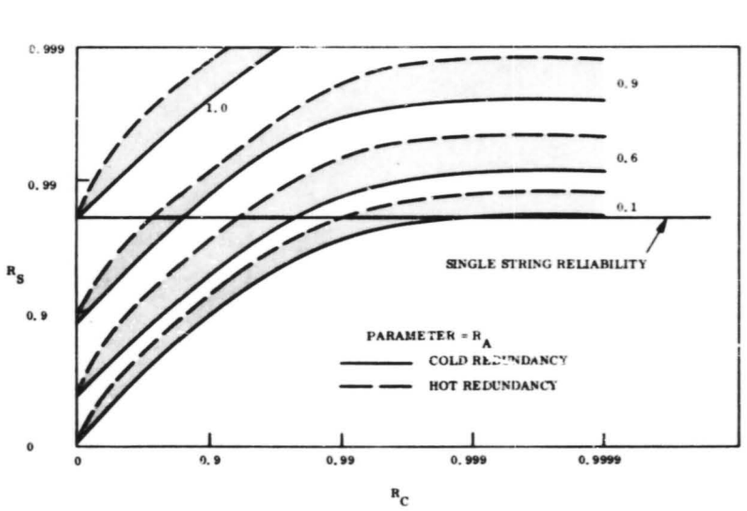
b. The failure modes of the fault sensing system included in "A" are frequently ignored in many analyses, and their importance is seen to be very significant.

c. There are many values of fault sensing reliability, R_A and R_c, which cause the redundant system to be less reliable than the single string system.

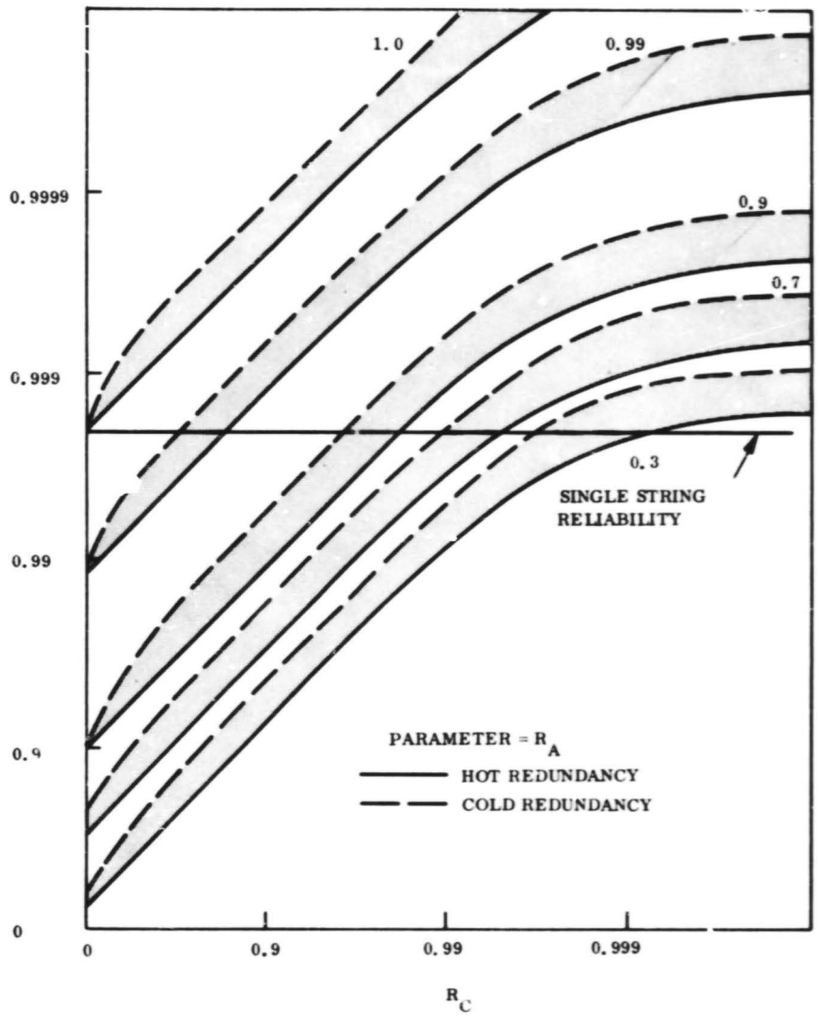
d. The improvement in system reliability for the cold case over the hot case is real, but not of large significance. The reliability of actual hardware for a cold system would be somewhere inbetween the hot and cold cases (the shaded region) since the hardware would be degrading to some extent even in the off condition, e.g., radiation damage to semiconductors.



PART A. $R_R = R_I = 0.9$



PART B. $R_R = R_I = 0.99$



PART C. $R_R = R_I = 0.999$

Figure 5.2.1-6. Cold Redundancy versus Hot Redundancy

e. Based on a, above, and Section 5.2.1.2.1, it is extremely important in implementing a switched redundancy system to assure that R_A and R_C are at least equal to R_R and R_I and that R_B is very high.

5.2.1.6 Split String vs Paired Switching

The regulator/inverter pair analyzed in the previous section could have been implemented in a split fashion such that if either the main regulator or the main inverter failed it would be switched out and the standby unit switched in and, then, when the remaining main unit failed its standby unit would be switched in. Figure 5.2.1-7, Part A, shows the basic split string being analyzed in this section and Figure 5.2.1-7, Part B, shows the corresponding block diagram used to assess the system reliability.

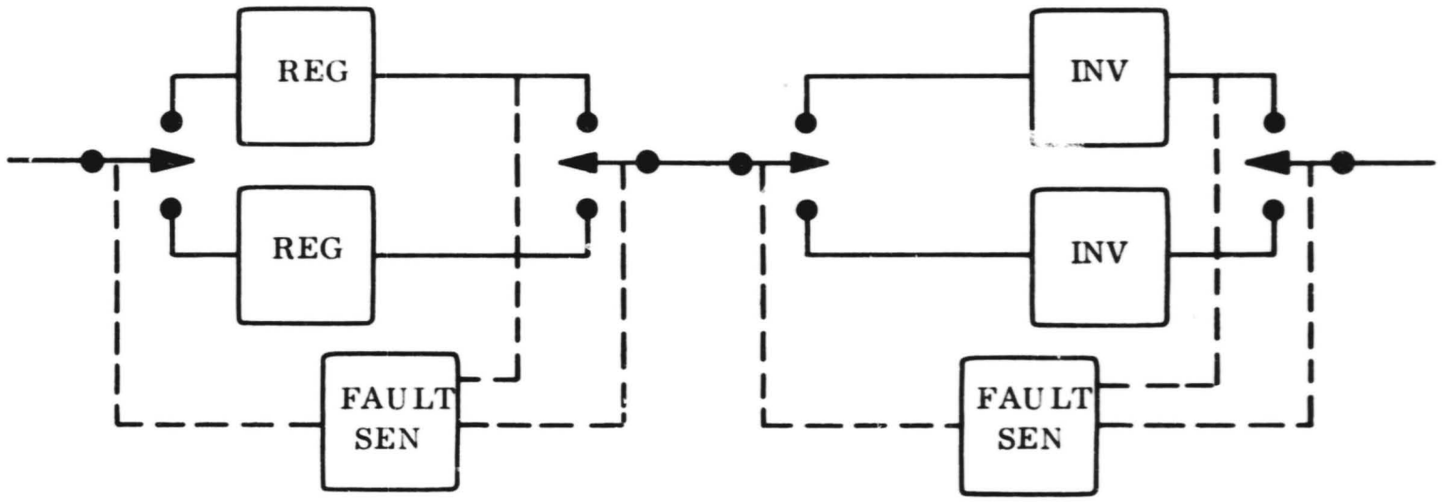
The analysis for this situation is performed on a hot redundancy basis and compared to the data in the previous section for a "paired" regulator and inverter (see Figure 5.2.1-5). The total split string system reliability is:

$$R_s = [1 - (1 - R_R R_A)(1 - R_R R_C)][1 - (1 - R_I R_A)(1 - R_I R_C)] R_B \qquad (5.2.1\text{-}5)$$

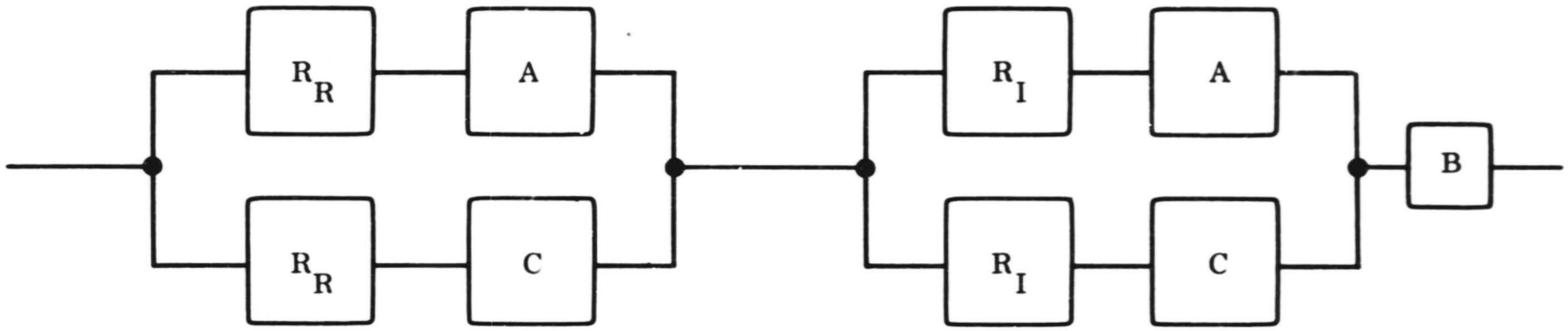
where the nomemclature is the same as in the previous sections.

Conclusions

Figure 5.2.1-8 shows the system reliability, R_s, versus the "C" reliability, R_c, with "A" as a parameter, R_A. The results of this section, the split string case, are shown as well as the paired regulator/inverter results from the previous section. The results are presented for three levels of black box reliability with Figure 5.2.1-8, Part A, being the lowest, $R_R = R_I = 0.9$ and Figure 5.2.1-8, Part C, being the highest, $R_R = R_I = 0.999$. The single string reliability of a single regulator and inverter is shown as a horizontal line. Also, as before, "B" is assumed perfect, hence, $R_B = 1.0$. Of course, the split string case "B" includes portions of an additional relay.

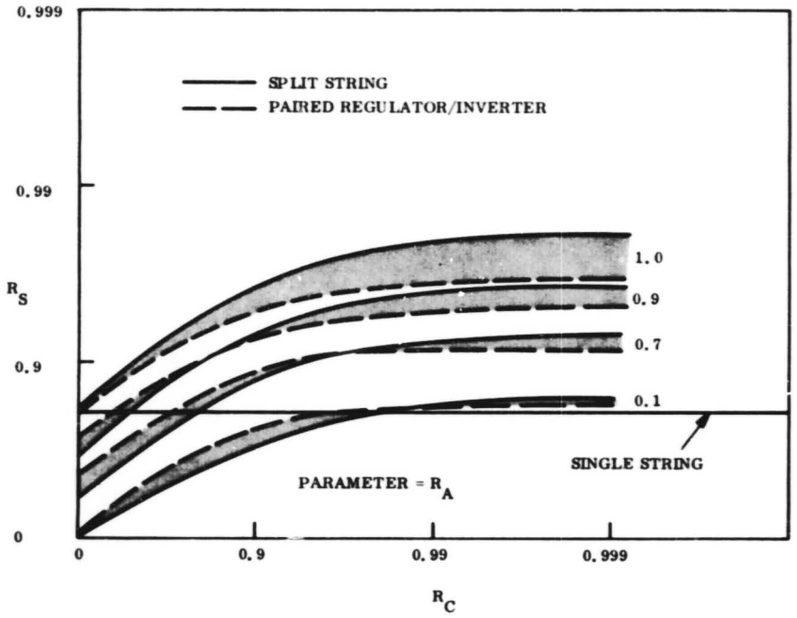


A

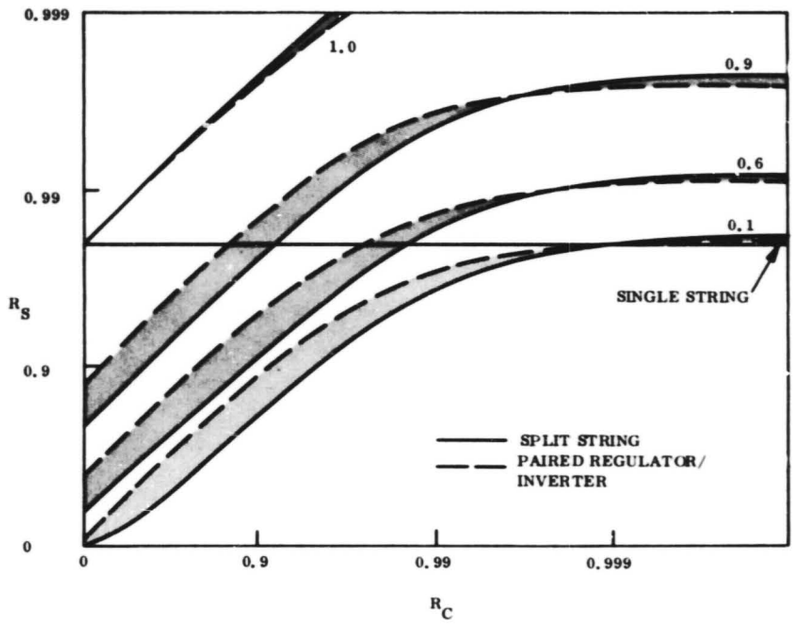


B

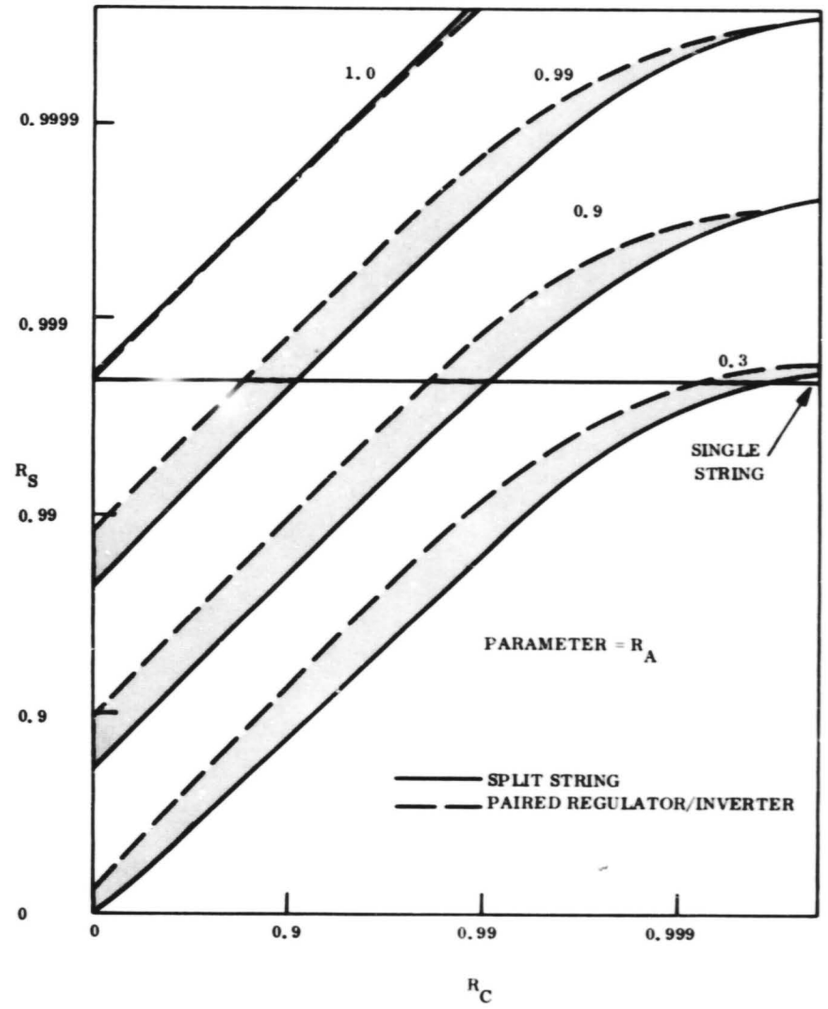
Figure 5.2.1-7. Split String Regulator/Inverter



PART A. $R_R = R_I = 0.9$



PART B. $R_R = R_I = 0.99$



PART C. $R_R = R_I = 0.999$

Figure 5.2.1-8. Split String versus Paired Regulator/Inverter

Examination of Figure 5.2.1-8 indicates the same general conclusions pertaining to the comparison of a single string system versus a switched redundant system as previously seen and only the specific conclusions from the comparison of the split string versus the paired regulator/inverter are listed below:

a. For low values of fault sensing reliability, R_A and R_C, the "paired" regulator/inverter system is more reliable than the split string approach.

b. For high values of fault sensing reliability, R_A and R_C, the split string system is most reliable.

c. The relative advantage of either system does not appear to be too significant, hence, the dominating consideration in choosing between approaches should be which system is easiest to implement so that the reliability of the "A" and "C" fault sensing hardware is highest.

5.2.1.7 Mariner Mars '69 Case

The Mariner Mars '69 regulator, inverter, and fault sensing were partially reviewed using the techniques discussed above. The failure rate data for functional elements were supplied by JPL* and are listed in Table 5.2.1-1. The circuit analyzed is shown in Figure 5.2.1-9 and the equation used is Equation 5.2.1-4. The results, for an assumed mission time of 5700 hours, are shown in Figure 5.2.1-10.

Table 5.2.1-1. Mariner Mars '69 Functional Element Failure Rates

Functional Element	Failure Rate (Per 10^6 Hours)	Reliability (Mission Time = 5700 Hours)
Regulator	5.76	0.968
Inverter	4.95	0.972
Failure Sensor, "C"	2.93	0.983
Relay, "B"	0.0085	0.99995

*Mariner Mars 1969 Flight Power Subsystem Design Review Report, Power Conditioning Equipment; Electro-Optical Systems Report No. 7178-DRR-002A, 17 April, 1967.

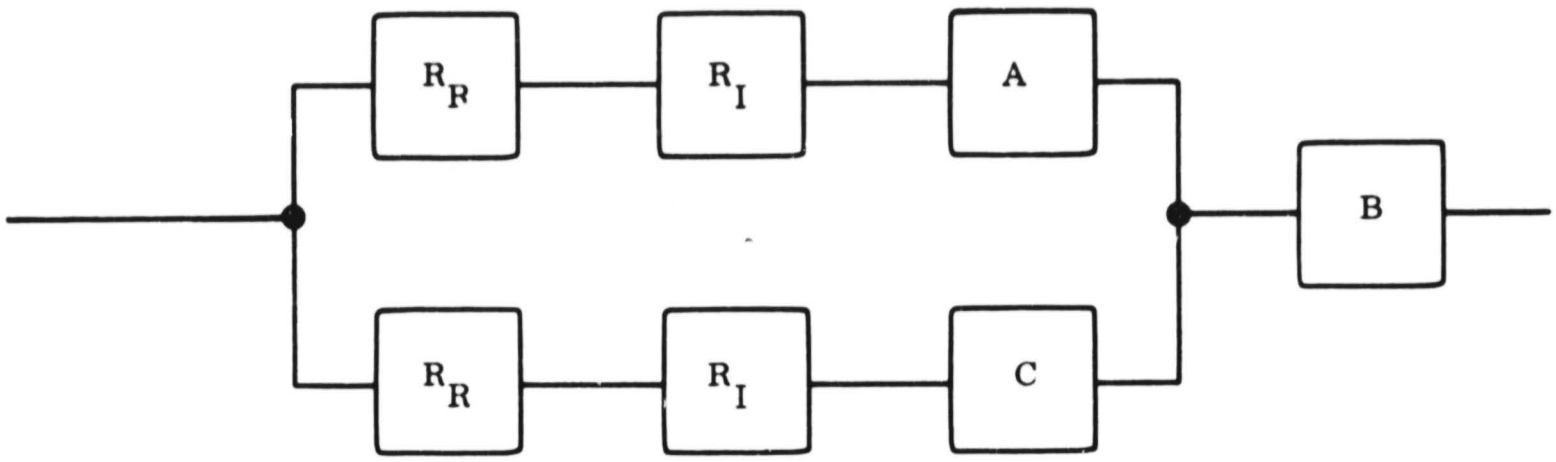


Figure 5.2.1-9. Mariner Mars '69 Regulator/Inverter/Fault Sensing

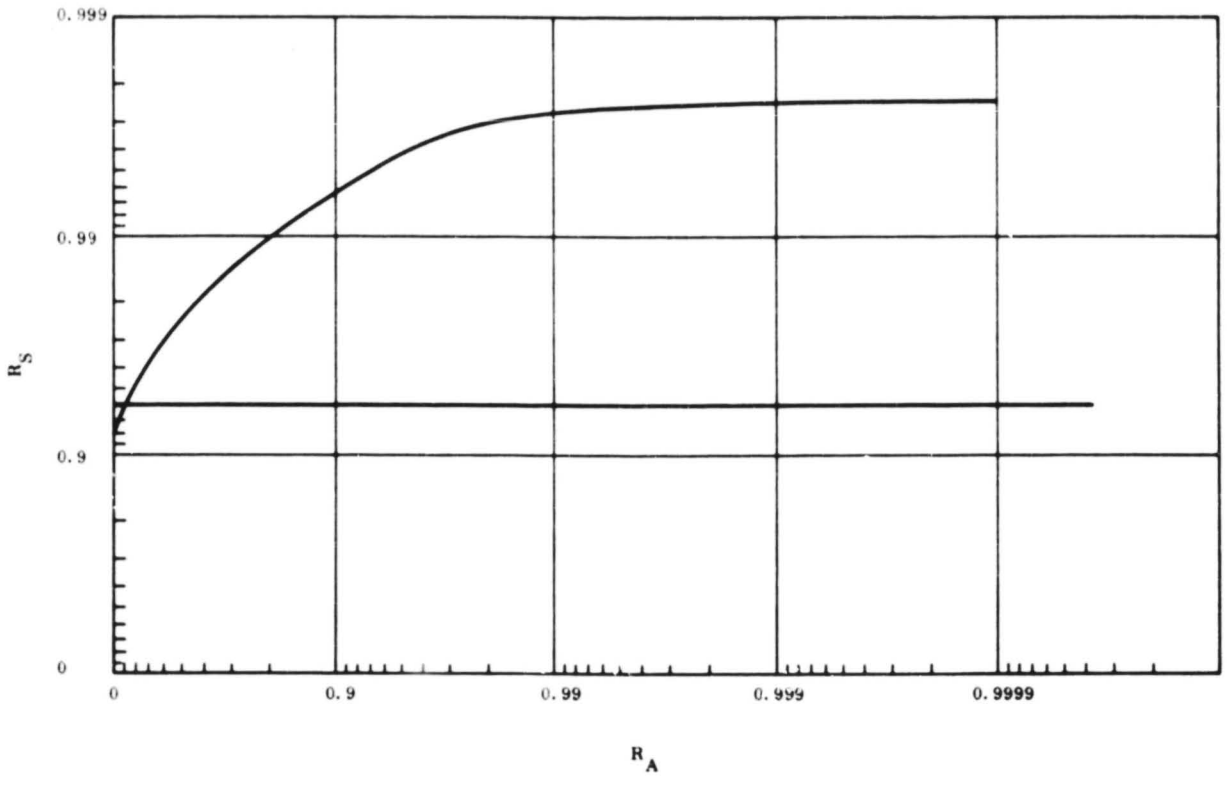


Figure 5.2.1-10. Mariner Mars '69 Regulator/Inverter/Fault Sensing

Analysis of the JPL supplied document did not identifv anything equivalent to the "A" block used in this study, hence the reliability was plotted versus R_A. Examination of Figure 5.2.1-10 indicates that the redundant system is better than the single string regulator/ inverter for any value of $R_A > 0.1$. This is the result we would expect, based on the conclusions of the previous sections, when the components have reliabilities as listed in Table 5.2.1-1. The question of how valid the component reliabilities really are, as pointed out in the introduction to Section 5.2.1, is very difficult to answer.

The analysis of this section is not completely representative of the actual MM '69 system. Additional work on this task, utilizing a more complete model of the MM '69 system, is discussed in Section 5.2.2 through 5.2.10.

5.2.1.8 General Conclusions/Recommendations

Table 5.2.1-2 presents a summary of the main conclusions reached from the reliability sensitivity studies to date.

Table 5.2.1-2. Summary of Main Conclusions

Question	Conclusion	Study Recommendation
In general, is fault sensing and switching of a standby element a good step?	It completely depends on the relative reliability of the main black boxes but as long as the fault sensing is comparable to the black boxes in reliability, then it is well worthwhile.	a. Review carefully the "A" block-which includes: 1. Hardware failures in the fault sensing which cause a false switching to the redundant chain, 2. Design of the level and duration of the fault criteria. If too tight, the system is more prone to false switch to the redundant chain. b. Assure that R_A and R_C, the fault sensing reliabilities, are equal to or greater than R_R and R_I, the regulator and inverter reliabilities.
Is separate fault sensing and switching of regulator and inverter better or worse than for the pair?	It depends: if R_A and R_C are low, no; if R_A and R_C are high, yes.	Relative improvement less than uncertainties of actual values of various elements, hence, other criteria should be used, such as: 1. Which approach is easiest to implement. 2. Which approach provides highest fault sensing reliabilities.
Where should effort be concentrated in overall power system to improve reliability?	For series elements always work on the element which is significantly lower than any other element. For parallel elements work on easiest element to improve.	a. Model MM '69 system and Shunt System- b. Perform sensitivity studies to identify which elements should be further improved.
Is the reliability improvement of cold redundancy over hot redundancy real?	Yes, however, it does not necessarily follow that the improvement is so great that it should always be used. That is, if some good engineering/reliability reason exists for using a hot redundancy situation, it might be worthwhile and should be studied.	Do not "blindly" be constrained by a cold redundancy requirement when designing the power components and subsystem.

5.2.2 RELIABILITY ANALYSIS METHODOLOGY

Reliability predictions for the various power subsystem configurations considered during the study were performed by using the Probability Calculator* portion of the Mission Expected Worth (MEW) computer program. The MEW program is an optimization technique developed by GE as part of the Voyager Task C studies for JPL. Optimization is accomplished by evaluating all possible system configurations resulting from alternative equipment designs and ranking them for mission worth based on any desired constraint such as weight, cost, schedule, etc.

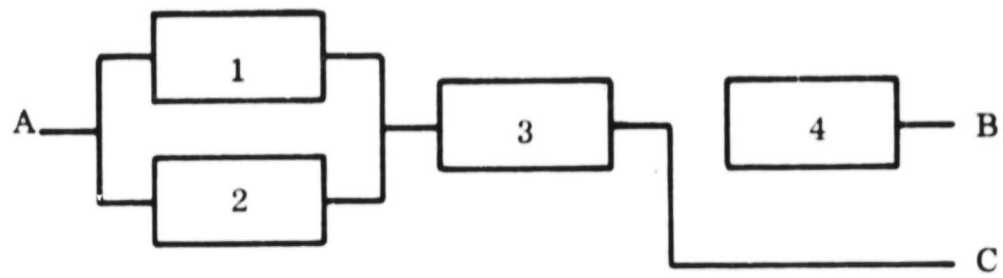
A vital input for the MEW analysis is the definition of all possible mission outcomes and the assignment of a mission worth or value to each of these outcomes. These value assignments are highly subjective and should be a systems-oriented task for a specific mission in order to achieve credible accuracy. Also, the use of a computerized method for optimizing system configuration makes it cumbersome to investigate the effect of subtle design changes. It was therefore decided early in this study not to use an automated approach for determining the recommended power system configuration. However, as indicated above, the Probability Calculator portion of the MEW program was used to facilitate reliability computations. In using this program, state transition diagrams and appropriate logic expressions are derived from a reliability block diagram and easily encoded for input to the computer. Other inputs are: Component Failure Rates, Mission Phases, and Stress Factors (failure rate multipliers) for each mission phase.

The computer sets up the differential equations defined by the state diagrams, carries out their solution by numerical methods, and performs the logic operations necessary to compute the probabilities of each output state. An example in use of this method follows.

Consider the following subsystem:

---

*The SIP Probability Calculator Program Source Deck, Program Listing, and Operating Instructions were transmitted to JPL during the study.



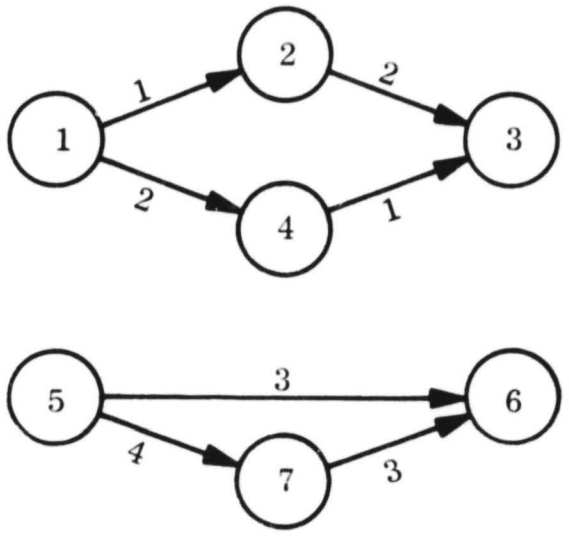
Components 1 and 2 are in a block redundant configuration. The failure of component 4 results in a degraded mission. Therefore, with a good input, B is the good output, and C is a degraded output.

Each entry under Mission Phase in Table 5.2.2-1 is the stress level multiplier for each component failure rate during each mission phase. The set of stress level multipliers across the entire mission is called a stress note, and is assigned a number.

Table 5.2.2-1. Mission Phases and Stress Time Profile

Component	Failure Rate (% / 1000 hrs)	Mission Phase						Stress Note No.
		1 (1 hr.)	2 (100 hr.)	3 (1000 hr.)	4 (1 hr.)	5 (1000 hr)	6 (10 hr.)	
1	0.84	10.0	1.0	1.0	10.0	1.0	0.1	1
2	0.84	10.0	1.0	1.0	10.0	1.0	0.1	1
3	1.12	10.0	0.1	1.0	1.0	1.0	1.0	2
4	0.78	10.0	0.1	0.1	10.0	0.1	1.0	3

5.2.2.1 State Transition Diagrams



Good States : 1, 2, 4, 5

Degraded States: 7

Failed States : 3, 6

To facilitate problem definition and computer input preparation, two separate state diagrams are defined as shown above. The circled numbers represent states and the numbers above the arrows are the component identification numbers. State 1 is an initial state and is defined as a good state. The arrow from state 1 to state 2 indicates the failure of component 1. Since components 1 and 2 are block redundant, the subsystem is still functioning after the failure of component 1, and state 2 is a good state. The arrow from state 2 to state 3 represents the failure of component 2 after component 1 has failed and 3 is therefore a failed state. Similarly, the arrow from state 1 to state 4 indicates the failure of component 2 with component 1 still operating and state 4 is therefore a good state. In the second diagram, state 5 is the initial good state. The arrow from state 5 to state 6 represents the failure of component 3, and 6 is therefore a failed state. The failure of component 4 results in a degraded state, 7, and the subsequent failure of component 3 results in failed state 6.

5.2.2.2 Logic Expressions

Subsystem Good : (① + ② + ④) x ⑤ = G

Subsystem Degraded : (① + ② + ④) x ⑦ = D

Subsystem Failed : ① - (G + D)

The above information is encoded for the computer, and a printout of selected input data and results for the example is shown in Figure 5.2.2-1.

5.2.3 MARINER '69 SINGLE STRING RELIABILITY ESTIMATE

Initially, a reliability prediction was computed for the single string (nonredundant) Mariner '69 power subsystem for use as a baseline.

```
                    NUMBER                                                  TM OPT
          SET       OF G+D   WEIGHT    POWER   VOLUME     COST FM TO
  I/A  NUMBER       STATES    (LBS)  (WATTS) (CU IN)     (DOL) PH PH I/A FAMILY NAME
  POA       4            2       0.       0.       0.       0.     1  6 SAMPLE PROBLEM

ANSWERS     3
     20        21        22

INITIAL CONDITIONS     2
      1 1.00000         2 1.00000

ARROWS     7

     STRESS NOTES AND FACTORS
          1          10.0   1.0   1.0  10.0   1.0   0.1
          2          10.0   0.1   1.0   1.0   1.0   1.0
          3          10.0   0.1   0.1  10.0   0.1   1.0

          RATE NO.        RATE          STRESS NOTE
      1         1          0.8400           1
      2         2          0.8400           1
      3         3          1.1200           2
      4         4          0.7800           3

     HEAD TAIL RATES (RATE NO.,TIMES USED(....)
          1    2    1       1    1
          2    3    1       2    1
          1    4    1       2    1
          4    3    1       1    1
          5    6    1       3    1
          5    7    1       4    1
          7    6    1       3    1

     HEAD TAIL  TRANSITION RATE
   1    2   8.4000
   2    3   8.4000
   1    4   8.4000
   4    3   8.4000
   5    6  11.2000
   5    7   7.8000
   7    6  11.2000

SUMS     1
   3  15         1         2         4

PRODUCTS     2
   2  20        15         5
   2  21        15         7

LOGICAL SUMS     1
   2  22         3         6

PHASE  TIME        GOOD          D1          FAILED          INTEGRATION INCREMENT   MATH FACTOR   ARROW FACTOR
   1      1.00  0.99981002  0.00007799  0.00011200          1.000                     0             1
   2    101.00  0.99961922  0.00015595  0.00022482
   3   1101.00  0.98763102  0.00092496  0.01144414          1000.000                  1             1
   4   1102.00  0.98754139  0.00100187  0.01145676          1.000                     1             1
   5   2102.00  0.97556277  0.00175173  0.02268551          1000.000                  1             1
   6   2112.00  0.97537713  0.00182762  0.02279525          10.000                    1             1
 ELAPSED COMPUTER TIME SINCE LAST TIME=     0.57
```

MISSION PROFILE

STORAGE LOCATIONS ASSIGNED TO OUTPUT STATES

STRESS FACTOR MULTIPLIERS FOR EACH MISSION PHASE

COMPONENTS USED IN MODEL

DEFINITION OF ARROWS AND RATES

LOGIC TO COMPUTE OUTPUT PROBABILITIES

STATE PROBABILITIES FOR EACH MISSION PHASE

Figure 5.2.2-1. Printout of Selected Data and Results

5.2.3.1 Reliability Block Diagram

The reliability block diagram for the Mariner '69 single string power subsystem is shown in Figure 5.2.3.1.

The following conditions were defined for this configuration:

a. There is an isolation diode (part of Power Source Logic) and a stack of six zener diodes in series associated with each of the 24 sections of the solar array. It is assumed that the loss of one isolation diode or one zener diode stack (or both for the same solar array section) will not affect system performance. This would result in the loss of one out of 24 solar array sections or 4.2 percent of capacity. It is assumed that the solar array design provides ample power capability to accommodate this small loss.

b. The battery consists of 18 cells in series. It is assumed that one shorted cell will result in degraded performance necessitating careful control of battery charging through ground command. An open cell will result in battery failure.

c. The failure of the inverter clock will cause a loss of frequency accuracy and will result in degraded performance.

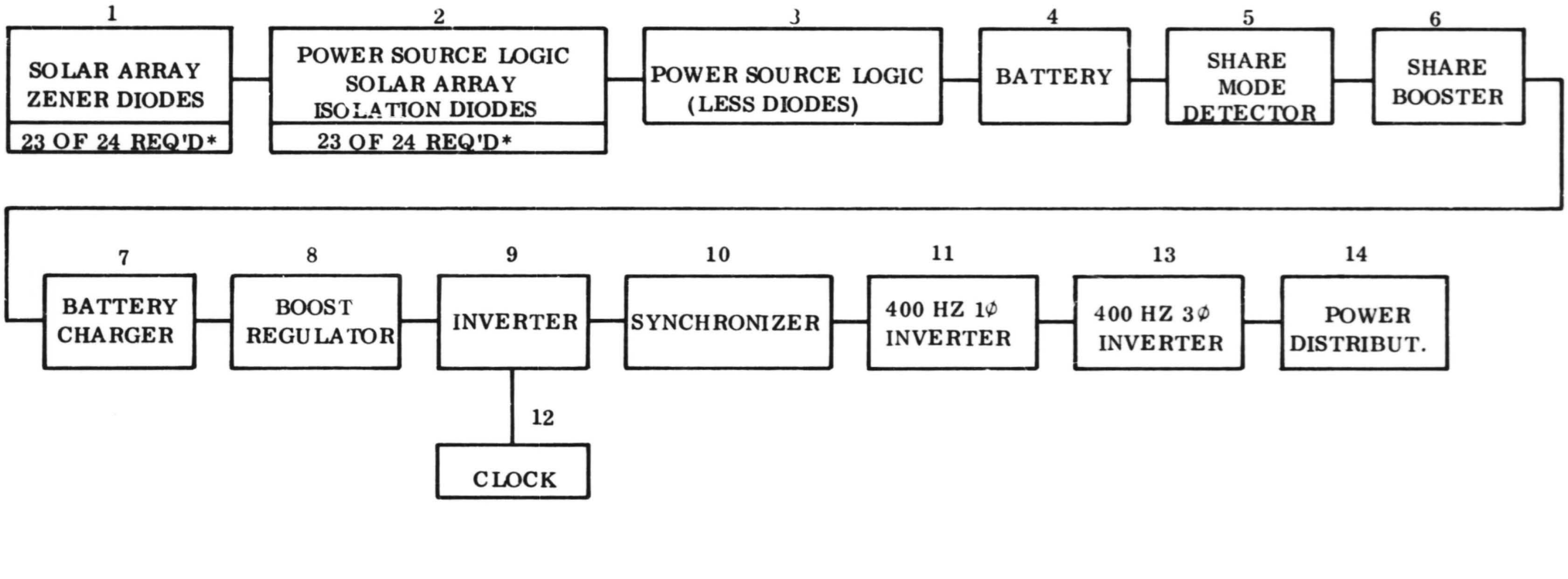
d. The solar array has not been included in this analysis.

e. Failures other than those listed in a, b, c, and d above will result in failure of the power subsystem.

5.2.3.2 Mission Profile

An assumed orbiter mission profile has been used as follows:

Mission Phase	Duration (Hr)
Prelaunch and Launch	1.1
Cruise	4320
Midcourse Maneuver (3)	4.2
Far Encounter	24
Orbit Insertion	1.6
Encounter Playback	3.1
Orbit	2160
Orbit Trim (2)	2.7
TOTAL MISSION TIME	6516.7 Hrs



* ALLOWABLE FAILURE OF ZENER AND ISOLATION DIODE ARE MUTUALLY EXCLUSIVE EXCEPT WHEN BOTH ARE ON SAME SOLAR ARRAY SECTION

Figure 5.2.3-1. Mariner '69 Power Subsystem Single String Configuration Reliability Block Diagram

This profile has been used for all analyses in this study.

5.2.3.3 Hardware Failure Rates

In order to perform a quantitative reliability analysis, it is necessary to assign failure rates to elements of the power subsystem. The subject of failure rates and failure distributions generally leads to endless and diverse discussion. The determination of highly accurate component failure rates (if at all possible) has not been considered a prime objective of this study. It was intended to evaluate the relative reliability of various configurations, and consider the results within the context of a group of decision criteria.

In those cases where differences in reliability values were small enough to be considered comparable to the accuracy of the prediction process, design decisions would be based largely on other considerations such as weight and efficiency. A reasonably consistent set of component failure rates would therefore yield sufficiently accurate results to consider estimated reliability of alternate configurations on a relative basis.

The hardware failure rates contained in the Electro-Optical Systems (EOS) Design Review Report (Reference 2) were initially established as a baseline. Reference 2 indicates that these values were obtained by using the minimum values in the Table of Part Class and Type Failure Rates (Table IV - IX) of MIL-HDBK-217A, and apparently assuming the conventional exponential failure distributions. Predictions were performed on several components using the above indicated failure rates, and then repeated using GE failure rates applicable to current space systems, (see Section 5.2.10.1). With few exceptions, the results indicated reasonable correlation. The use of failure rates projected for the 1973-1975 period would obviously result in higher reliability estimates, but they would not appreciably alter the ranking of alternate configurations, and they lack credence in considering current systems.

With due consideration for the accuracy of the prediction process, it was decided to use the EOS failure rates in analysis of the existing power subsystem. Failure rates for new designs (discussed in subsequent paragraphs) employ the MIL-HDBK-217A part failure rates in order to provide a consistent prediction for relative evaluation.

The failure rates used and the stress level multipliers for each mission phase are given in Table 5.2.3-1. Two assumptions are made with respect to the stress level multipliers:

Table 5.2.3-1. Mariner '69 Power Subsystem Failure Rates and Stress Levels for Each Mission Phase

Item	Failure Rate (%/1000 hr)	Mission Phase							
		1	2	3	4	5	6	7	8
Boost Regulator	0.586	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Inverter	0.20	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Clock	0.295	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Battery Cell - Open	0.00689	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Battery Cell - Short	0.06871	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Power Source Logic Isolation Diode	0.01	0.1	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Power Source Logic	0.08855	0.1	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Zener Diode Stack	0.18	0.6	0.1	0.4	0.1	0.6	0.1	0.1	0.5
Synchronizer	0.51785	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Share Mode Detector	0.181	0.6	0.125	1.0	1.0	0.1	0.1	0.16	0.1
Share Booster	0.438	1.0	0.125	1.0	1.0	0.1	0.1	0.16	0.1
Battery Charger	0.30	0.1	0.125	1.0	1.0	0.1	0.1	0.16	0.1
Power Distribution	0.616	0.13	1.0	1.0	1.0	1.0	1.0	1.0	1.0
400 Hz, 1ϕ, Inverter	0.08685	0.1	0.1	0.1	1.0	0.1	0.1	1.0	0.1
400 Hz, 3ϕ, Inverter	0.05585	1.0	1.0	1.0	0.1	1.0	0.1	0.1	1.0
*Failure Detector (Prime)	0.20595	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
*Failure Detector (Backup)	0.08885	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

*Used in Redundant Configuration Only (see Section 5.2.4.1 b)

a. Equipment which is in a nonoperating state (i.e., turned off during selected mission phases or standby redundant units) is considered to have one-tenth the failure rate of the same unit when in an operating state. Supporting data is presented in Section 5.2.10.2.

b. High value multipliers were not used for the launch, midcourse maneuvers, orbit insertion, and orbit trim phases. These multipliers generally range from 2 to 100. The actual period during which the spacecraft is subjected to the higher stress levels is less than one hour in a mission duration of approximately 6500 hours. Assuming an average multiplier of 50, the worst case error is less than 3 percent and does not appear to justify the additional computation complexity required to establish and use these factors.

5.2.3.4 Results

The prediction was obtained using the method described in Section 5.2.2 with results as follows:

Probability of no subsystem failure	=	0.7766
Probability of Degraded Mode 1 (clock failure)	=	0.0151
Probability of Degraded Mode 2 (1 battery cell shorted)	=	0.0627
Probability of Mission Failure	=	0.1444

The two values of significance here are the first one (0.7766) which is the probability that the subsystem is good for the entire mission, and the complement of the last figure (1-0.1444 = 0.8556) which is the probability that the subsystem does not fail completely.

5.2.4 MARINER '69 REDUNDANT POWER SUBSYSTEM RELIABILITY ESTIMATE

A reliability prediction was next performed on the basic Mariner 69 subsystem with block redundant boost regulator and inverter.

5.2.4.1 Reliability Block Diagram

The reliability block diagram for this configuration is given in Figure 5.2.4-1. All of the conditions stated in Section 5.2.3.1 apply here with the following exceptions and additions:

a. In the event of an inverter clock failure when the subsystem is operating in the prime mode, the subsystem will switch to the backup mode. If there is an inverter clock failure when the subsystem is operating in the backup mode, degraded performance will result due to loss of frequency accuracy.

b. The failure detector has been split into two sections. The portion assigned to the prime mode consists of those items which, if they fail, would cause the subsystem to switch to the backup mode. The portion assigned to the backup mode consists of those items whose failure would make it impossible to switch to the backup mode if a failure occurred in the prime units.

5.2.4.2 Mission Profile

The assumed orbiter mission profile given in Section 5.2.3.2 was also used for this analysis.

5.2.4.3 Hardware Failure Rates

The failure rates used for this configuration are given in Table 5.2.3-1. The same conditions stated in Section 5.2.3.3 apply here with the following addition:

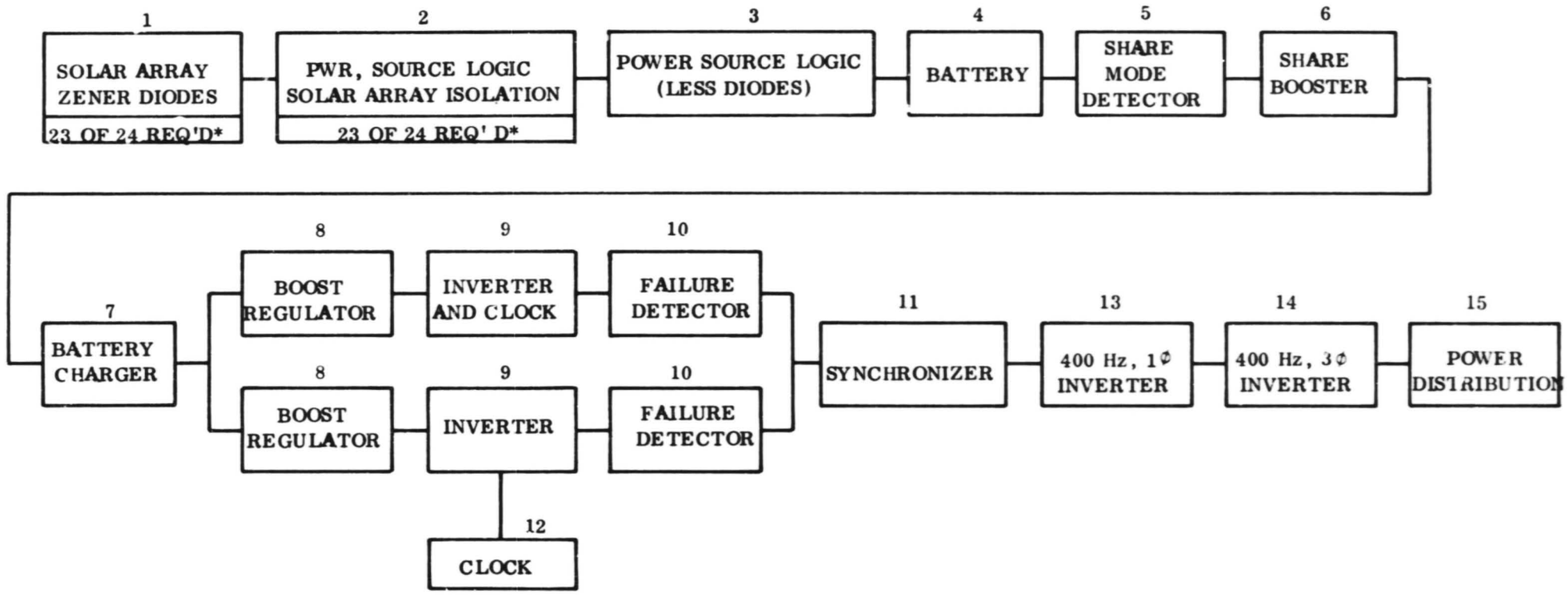
The split of the failure detector into prime and backup units was accomplished by a failure mode and effect analysis on the failure detector circuitry at the piece part level (see Section 5.2.10.3).

5.2.4.4 Reliability Sensitivity Studies

In order to determine the areas most sensitive to reliability improvement, each component failure rate in turn was reduced by a factor of 10 while holding the remaining failure rates at their initial values. The subsystem reliability was then recalculated for each case. The results are plotted in histogram form in Figure 5.2.4-2. The crosshatched area in each bar on the histogram is the probability of the subsystem being in a fully operational state for the entire mission. The blank area is the probability of being in a degraded state, and therefore, the complete bar is the probability of the subsystem not failing. The results are discussed in the following section.

5.2.4.5 Results

The initial prediction was obtained using the method described in Section 5.2.2 with results as follows:



*ALLOWABLE FAILURE OF ZENER AND ISOLATION DIODE ARE MUTUALLY EXCLUSIVE EXCEPT WHERE BOTH ARE ON SAME ARRAY SECTION

Figure 5.2.4-1. Mariner '69 Power Subsystem Redundant Configuration Reliability Block Diagram

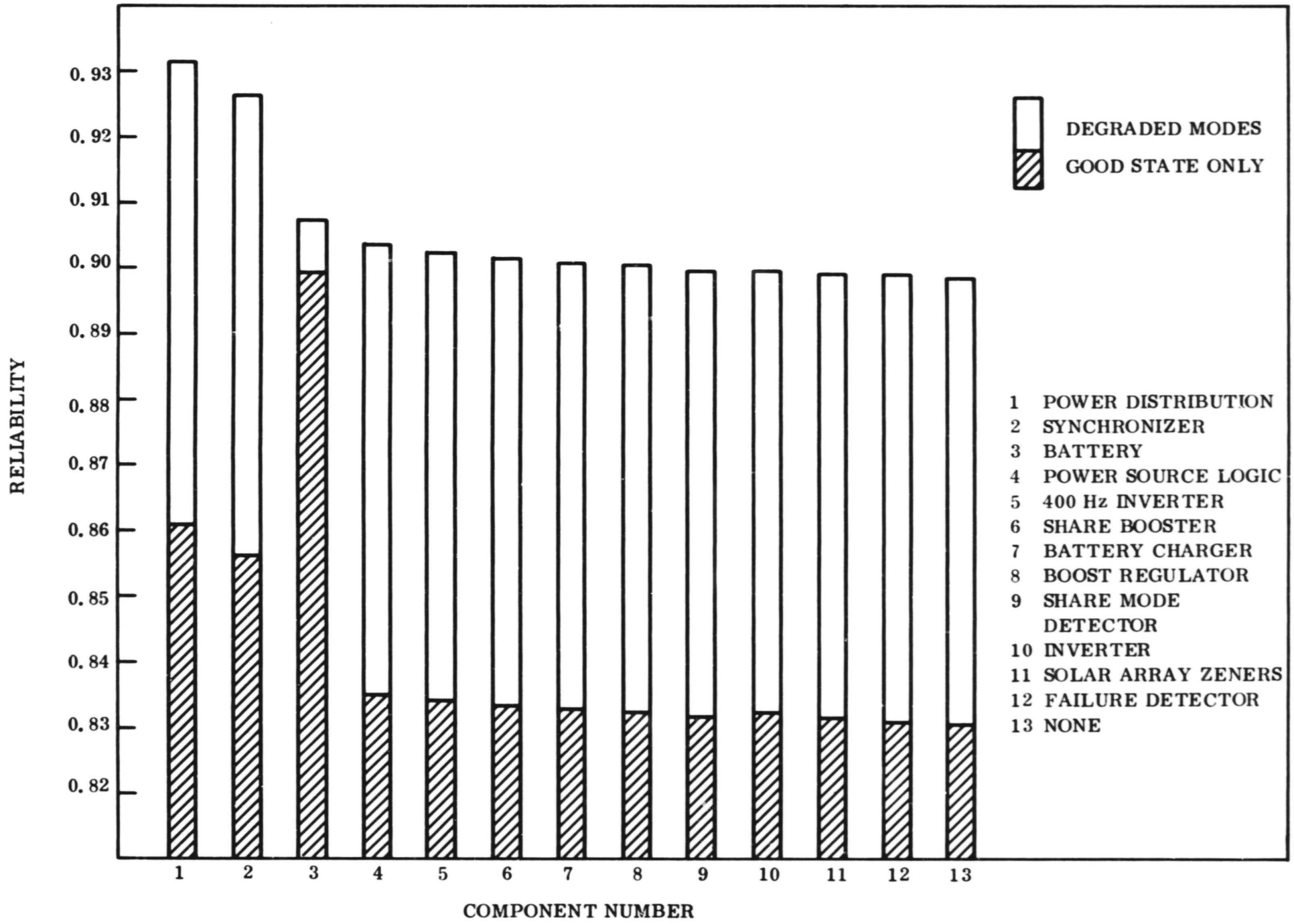


Figure 5.2.4-2. Reliability Resulting from 10 to 1 Improvement in Failures of Indicated Component-Redundant Power Subsystem

Probability of no subsystem failure	=	0.8305
Probability of Degraded Mode 1 (clock failure)	=	0.0007
Probability of Degraded Mode 2 (1 battery cell shorted)	=	0.0671
Probability of Mission Failure	=	0.1016

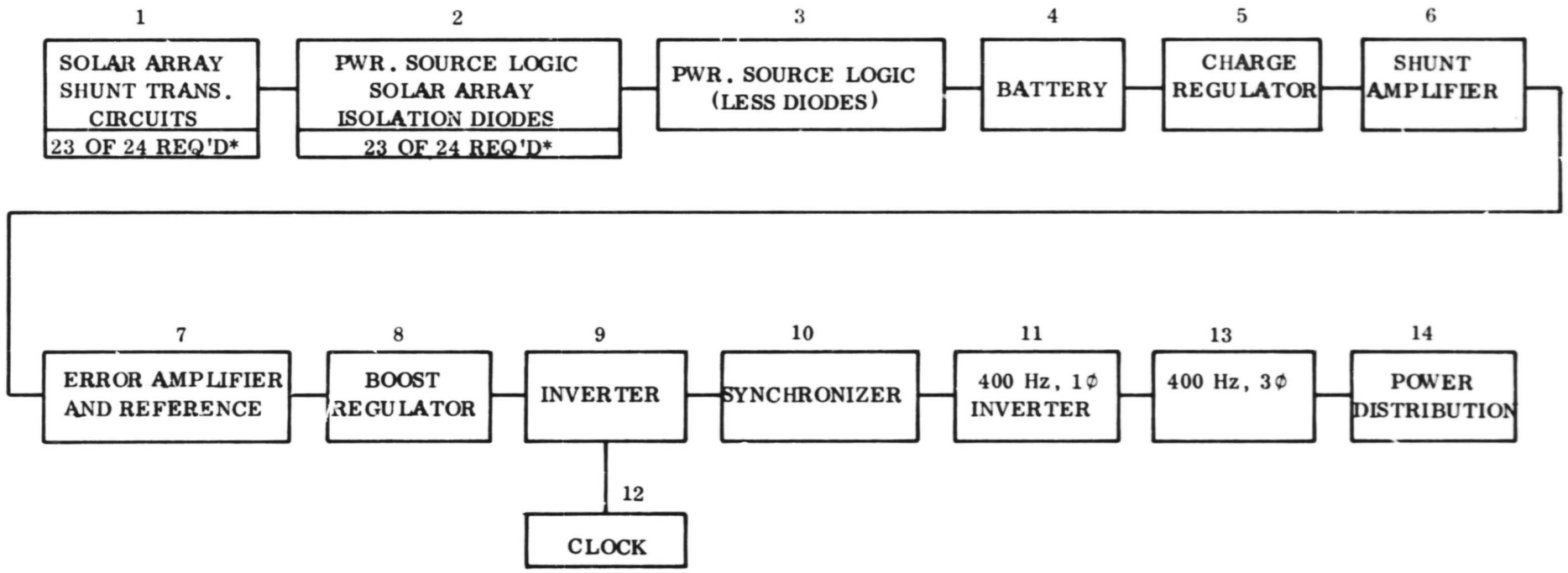
The two values of significance here are the first one (0.8305) which is the probability that the subsystem is good for the entire mission, and the complement of the last figure (1 - 0.1016 = 0.8984) which is the probability that the subsystem does not fail completely.

A review of the sensitivity data, Figure 5.2.4-2, indicates that the most significant improvements can be accomplished by improving the reliability of the power distribution section, the synchronizer, and the battery.

The power distribution section consists largely of relay drivers and relays to activate the science functions. As indicated previously, it has been assumed that any failure in the power distribution results in subsystem failure. A detailed analysis at the system level would probably reveal a number of permissible failures resulting in degraded modes of operation, thus reducing the contribution of the power distribution to subsystem reliability. Possible approaches to reliability improvement of the power distribution elements are discussed in Sections 5.1.3 and 5.2.9.2. Some of these same approaches are applicable to the Power Source Logic module.

Improvement in synchronizer reliability appears possible by turning it off during those mission phases where the 400 Hz inverter is not required. This approach was adopted for the shunt system and is discussed in subsequent sections of this report.

The battery reliability impinges on state of the art considerations and is discussed in Section 5.3.2.



*ALLOWABLE FAILURE OF SHUNT TRANSISTOR CIRCUIT AND ISOLATION DIODE ARE MUTUALLY EXCLUSIVE EXCEPT WHEN BOTH ARE ON SAME ARRAY SECTION

Figure 5.2.5-1. Mariner Power Subsystem Single String Shunt System Reliability Block Diagram

5.2.5 SHUNT SYSTEM SINGLE STRING RELIABILITY ESTIMATE

Preliminary studies indicated that a shunt regulator system is a prime candidate for optimum power subsystem design. A reliability estimate was therefore computed for a single string (nonredundant) shunt system for use in subsequent trade studies.

5.2.5.1 Reliability Block Diagram

The reliability block diagram for the single string shunt system is given in Figure 5.2.5-1.

The assumptions given in Section 5.2.3.1 for the M '69 single string subsystem also apply to the shunt system with one exception:

> The zener diodes are not used in the shunt system. However, the assumption relative to the zener diodes applies to the shunt transistors, i.e., the loss of one shunt transistor or one isolation diode (or both associated with the same solar array section) is tolerable and will not affect system performance.

5.2.5.2 Mission Profile

The assumed orbiter mission profile given in Section 5.2.3.2 was used for this analysis.

5.2.5.3 Hardware Failure Rates

The failure rates and the stress levels for each mission phase used for this analysis are given in Table 5.2.5-1. The same conditions stated in Section 5.2.3.3 relative to failure rates apply for this analysis. It is noted that provision has been made for turning the synchronizer off during those periods when it is not required, as suggested by the results discussed in Section 5.2.4.5.

This approach raises the question of the relative reliability of equipment which is operated continuously compared with cycled operation. This subject requires further investigation.

Table 5.2.5-1. Shunt System Failure Rates and Stress Levels for Each Mission Phase

Item	Failure Rate (%/1000 hr)	Mission Phase							
		1	2	3	4	5	6	7	8
Boost Regulator	0.57685	1.0	0.4	1.0	0.154	1.0	1.0	0.102	1.0
Inverter	0.2017	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Clock	0.295	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Shunt Amplifier	0.09085	0.1	0.7	0.1	0.946	0.1	1.0	0.999	0.1
Error Amplifier and Reference	0.21285	0.1	0.7	0.1	0.946	0.1	1.0	0.999	0.1
Battery Cell-Open	0.00689	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Battery Cell-Short	0.06871	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Charge Regulator	0.3117	0.1	0.125	1.0	1.0	0.1	0.1	0.16	0.1
Power Source Logic Isolation Diode	0.01	0.1	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Power Source Logic	0.08685	0.1	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Shunt Transistor Circuit	0.017	0.1	0.7	0.1	0.946	0.1	1.0	0.999	0.1
Synchronizer	0.5287	1.0	0.1	1.0	1.0	1.0	0.1	0.175	1.0
400 Hz, 1Φ, Inverter	0.08685	0.1	0.1	0.1	1.0	0.1	0.1	0.175	0.1
400 Hz, 3Φ, Inverter	0.05585	1.0	0.1	1.0	0.1	1.0	0.1	0.175	1.0
Power Distribution	0.616	0.13	1.0	1.0	0.1	1.0	1.0	1.0	1.0
*Failure Detector	0.481	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
* Failure Detector (Backup)	0.48002	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0

*Used Only In Redundant Configuration

5.2.5.4 Results

The reliability prediction for the single string shunt system was as follows:

Probability of no subsystem failure	=	0.8163
Probability of Degraded Mode 1 (clock failure)	=	0.0158
Probability of Degraded Mode 2 (1 battery cell shorted)	=	0.0659
Probability of Mission Failure	=	0.1006

5.2.6 SHUNT SYSTEM REDUNDANCY TRADE STUDY (BIA)

A brief review of the shunt system functional element failure rates and operating times indicated that the most fruitful areas for redundancy from the point of view of both potential reliability improvement and technical (design) implementation were the following:

Inverter (I)

Boost Regulator (B)

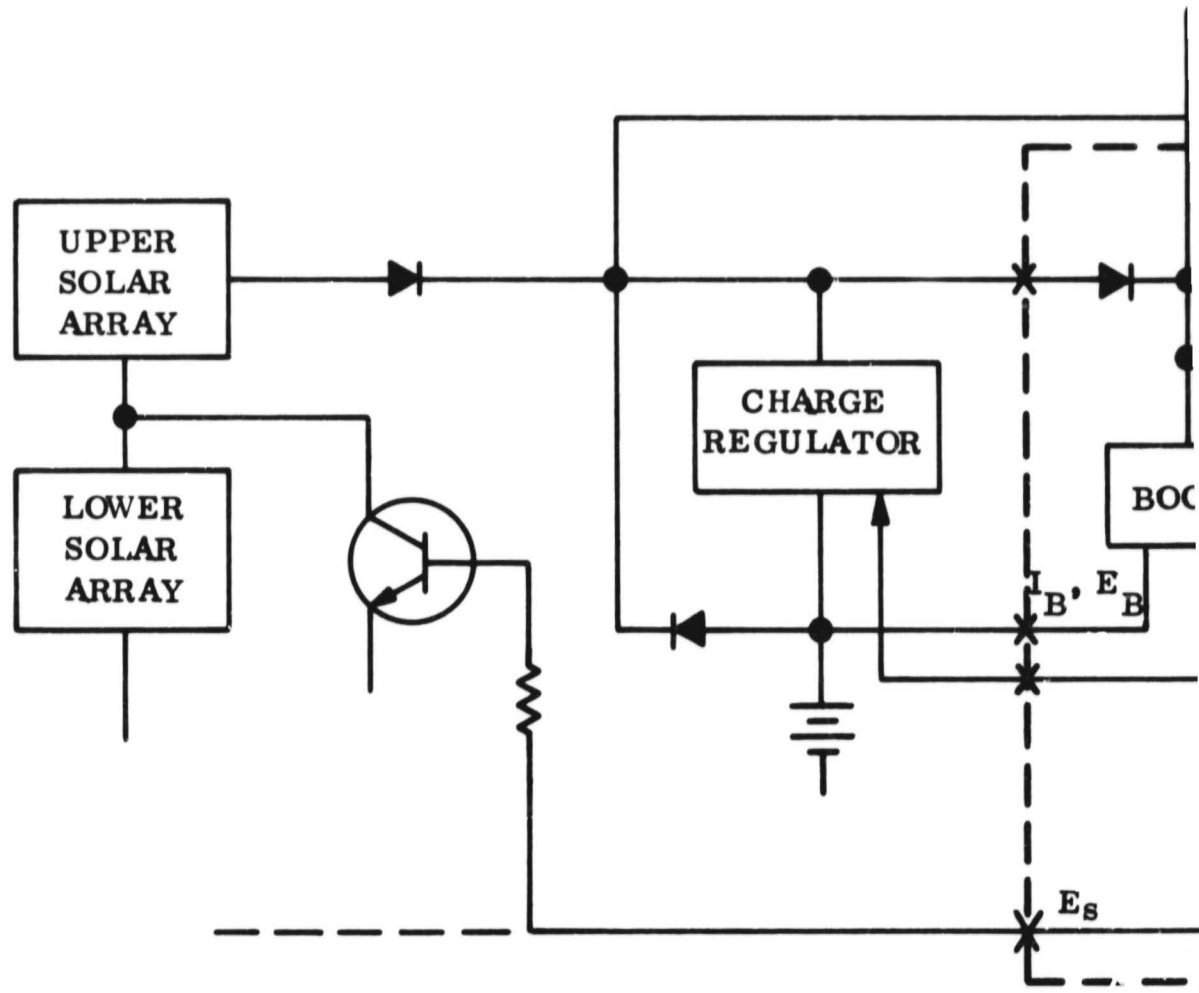
Shunt Amplifier (including Error Amplifier and Reference) (A)

The redundancy scheme for the Boost/Inverter/Amplifier (BIA) group described in Section 4.4.1 was based on a comparative study of several alternative approaches. These alternatives considered the principal boost, inverter, and amplifier functions taken singly or in a combination that could be arranged with block redundancy implementation. The purpose of this study was to assess the potential reliability gain of switching separate rather than grouped functions in the event of failure. The discussion of single versus split string reliability provided some of the incentive in this investigation (Section 5.2.1).

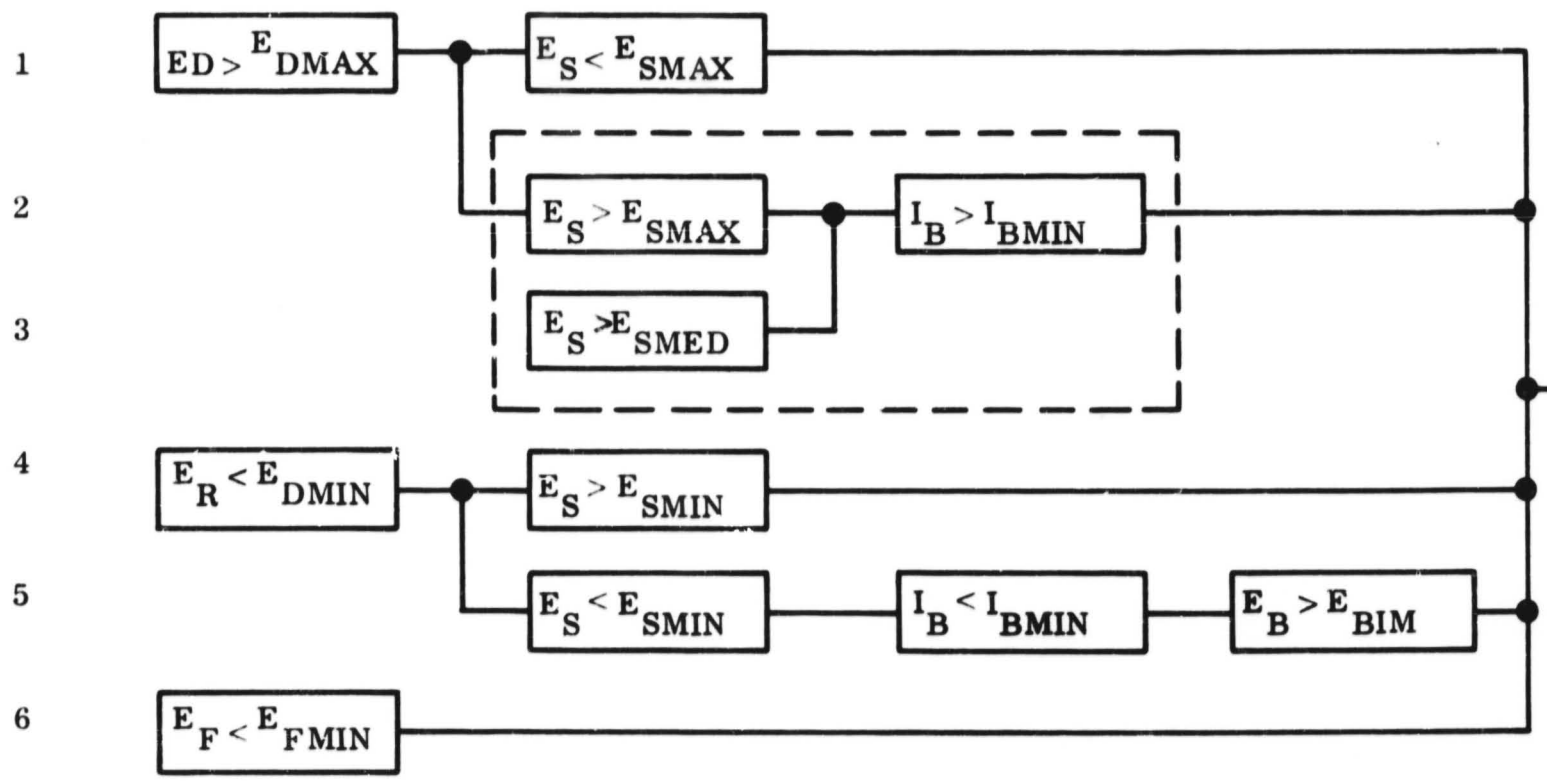
The several cases examined are described in the following paragraphs.

5.2.6.1 Case I - See Figure 5.2.6-1

The functions are combined with a single block which is replaced by an identical block upon any internal failure. The dotted line defines the block, and the line intersections define the switching points to an identical block.



COMPLETE FAULT SENSOR LOGIC



FOLDOUT FRAME

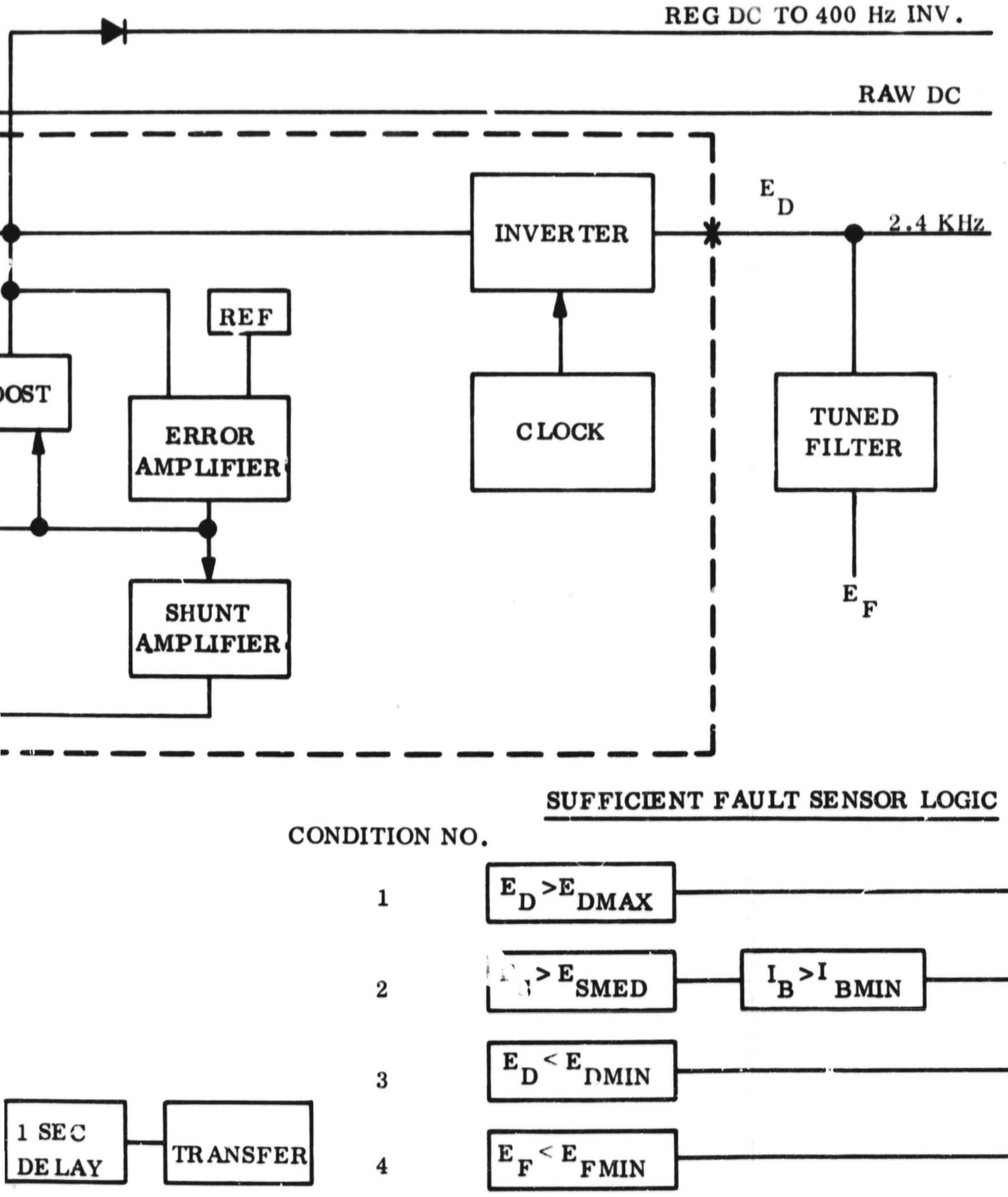
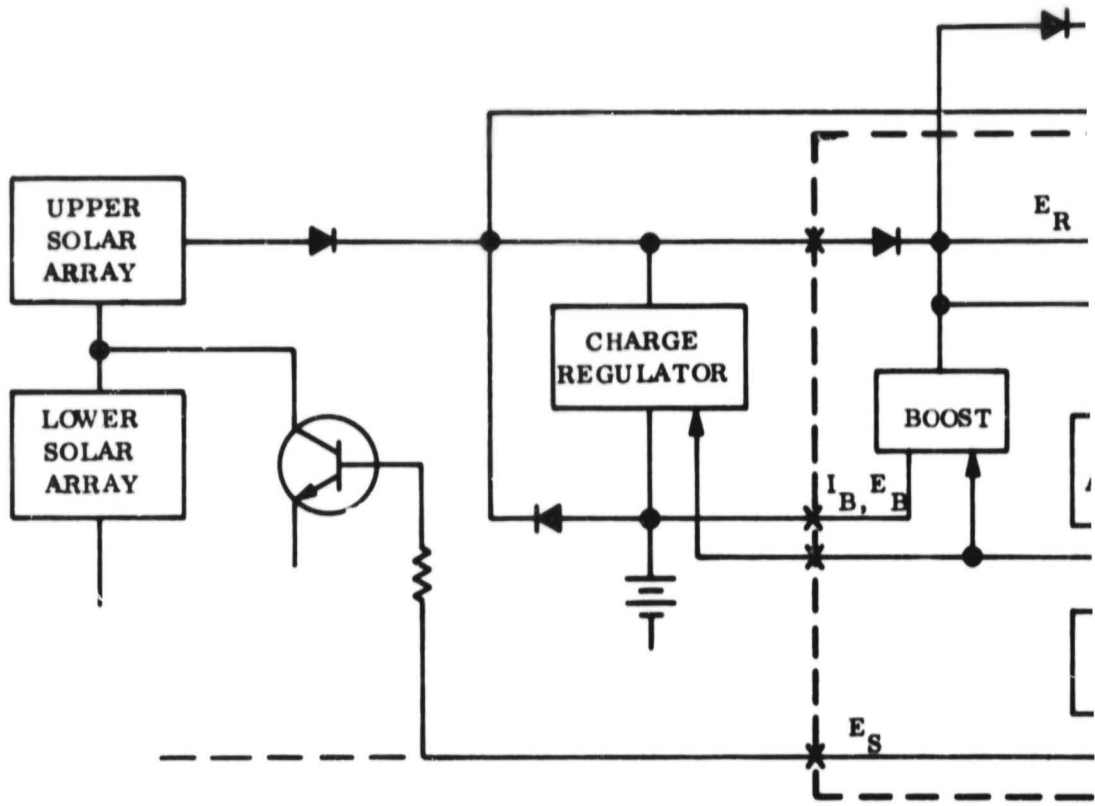
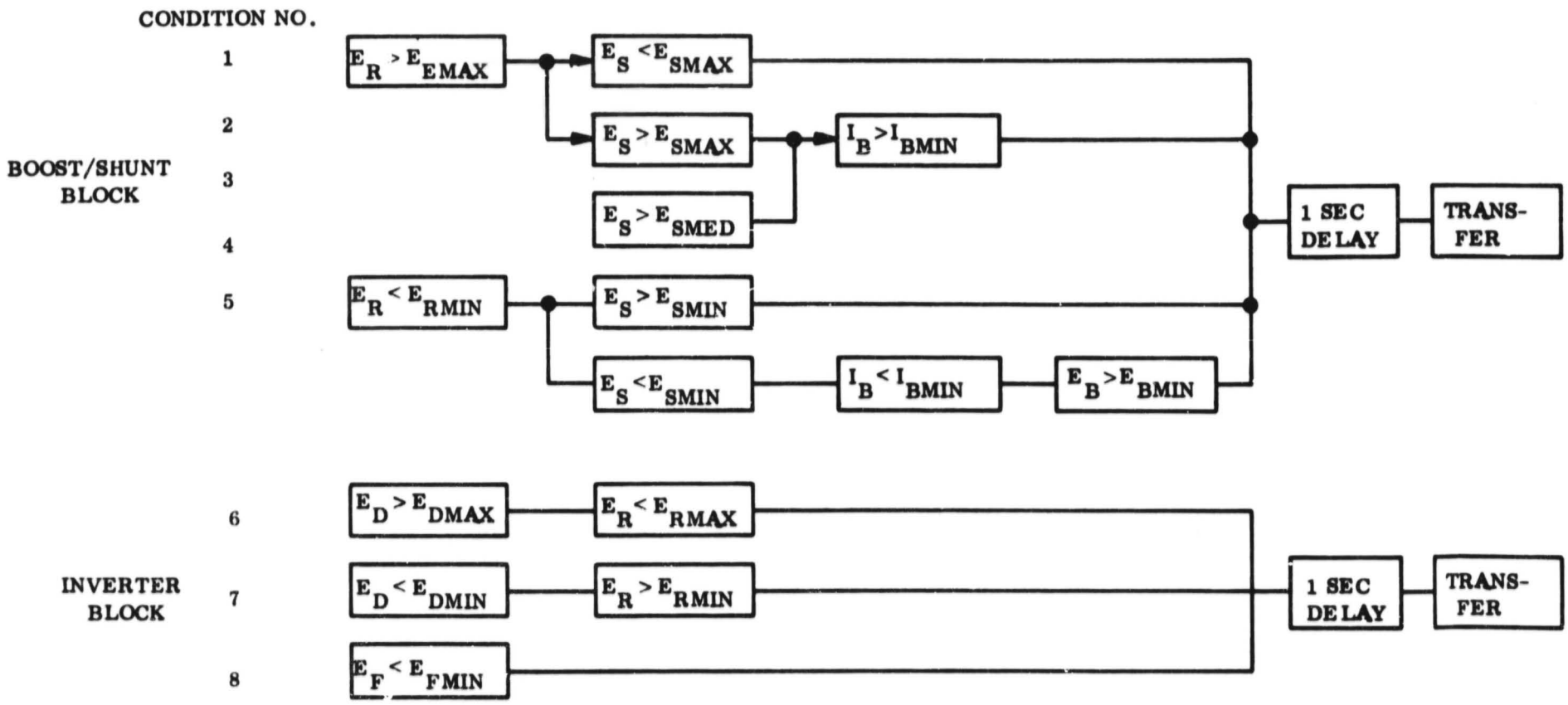


Figure 5.2.6-1. Case I - Boost/Inverter/ Amplifier Group, Single Block Redundancy

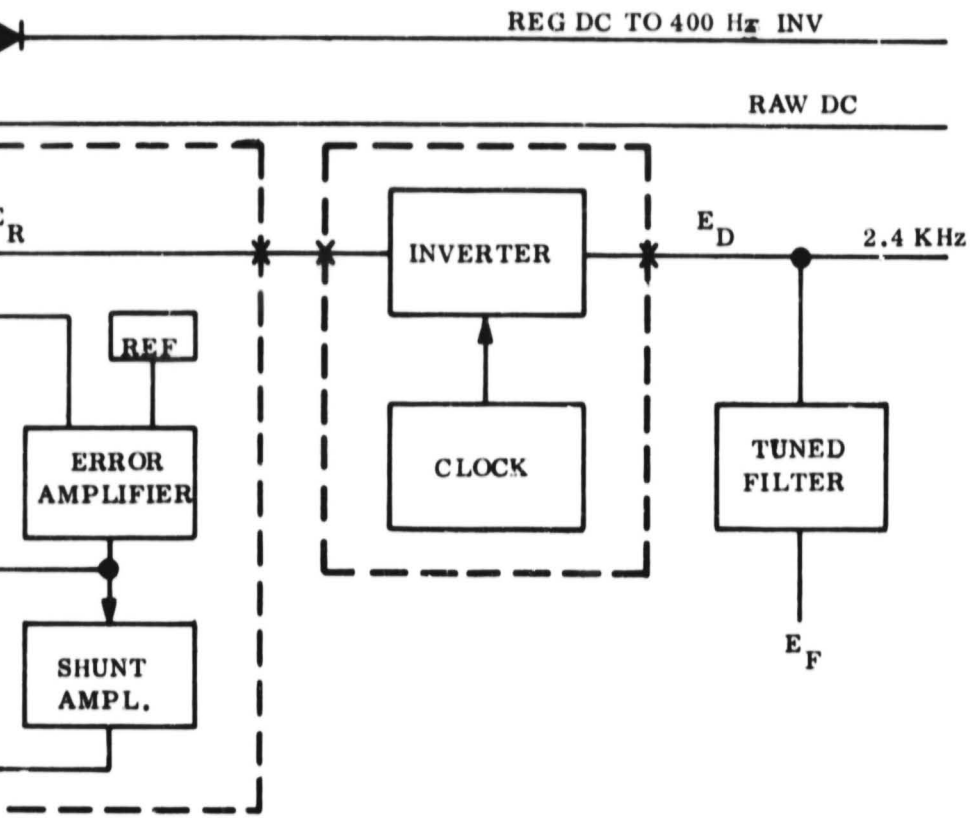
FOLDOUT FRAME 2



COMPLETE FAULT SENSOR LOGIC



FOLDOUT FRAME 1



CONDITION NO. SUFFICIENT FAULT SENSOR LOGIC

1 $E_R > E_{RMAX}$ AND $E_S < E_{SMAX}$

2 $E_S > E_{SMAX}$ AND $I_B > I_{BMIN}$

3 $E_S > E_{SMED}$

4 $E_R < E_{RMIN}$ AND $E_S > E_{SMIN}$

5 $E_S < E_{SMIN}$ AND $I_B < I_{BMIN}$ AND $E_B > E_{BMIN}$

1 SEC DELAY → TRANSFER

6 $E_D > E_{DMAX}$ AND $E_R < E_{RMAX}$

7 $E_D < E_{DMIN}$ AND $E_R > E_{RMIN}$

8 $E_F < E_{FMIN}$

1 SEC DELAY → TRANSFER

Figure 5.2.6-1. Case II - Boost/Inverter/ Amplifier Group, Double Block Redundancy

FOLDOUT FRAME 2

5.2.6.2 Case II - See Figure 5.2.6-2

The functions are combined into two switchable blocks: one contains the boost regulator, error amplifier, and shunt amplifier; the second contains the inverter and clock.

5.2.6.3 Case III - See Figure 5.2.6-3

The functions are combined into two switchable blocks: one contains the boost retulagor, inverter, and clock; the second contains the error amplifier and shunt amplifier.

More complex arrangements were considered, e.g., three switchable blocks, but analysis was deferred pending results on the above cases.

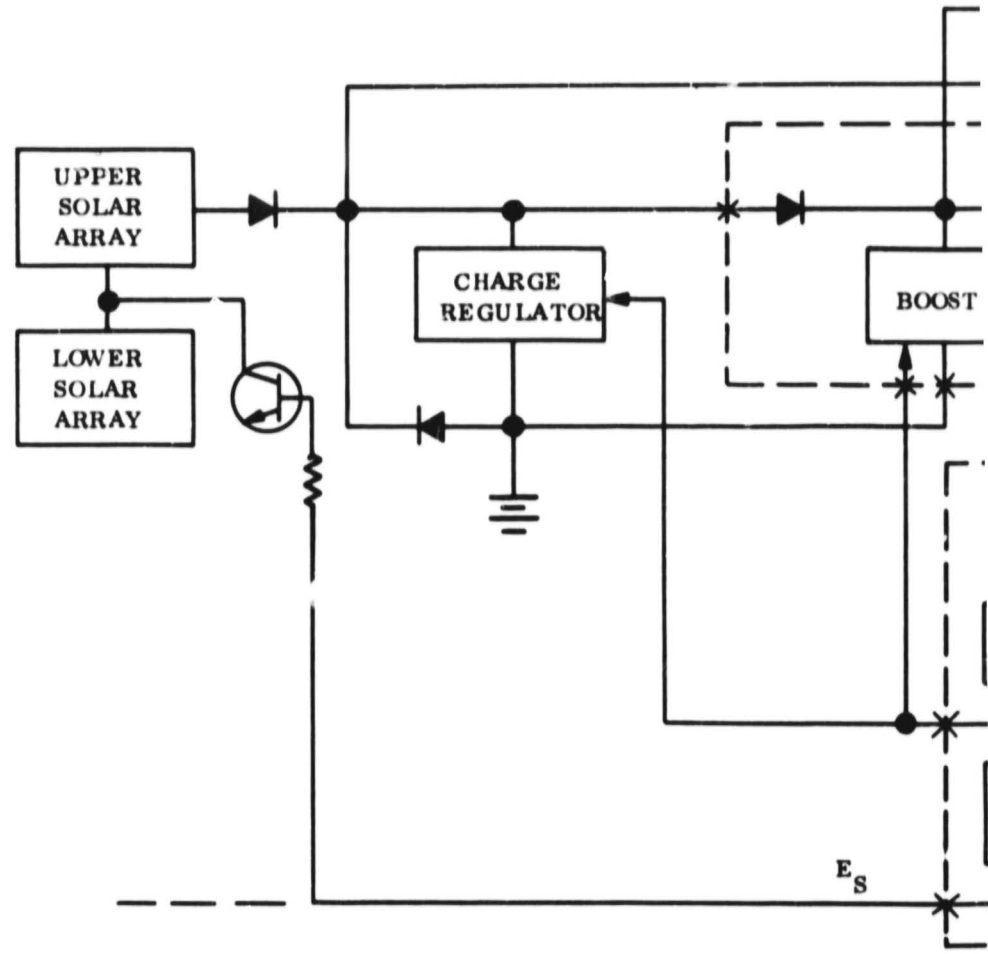
Fault sensor logic was prepared for each case as shown on each figure. The left-hand logic diagram constitutes a complete definition of fault sensor requirements which differentiates between internal and external faults; the right-hand diagram is an abridged, though sufficient, definition. An explanation of these diagrams is described in the following paragraphs for Case I.

5.2.6.3.1 Complete Fault Sensor Definition

Measures of performance are provided by:

- E_D - Distributed 2.4 kHz voltage
- E_S - Shunt amplifier voltage
- I_B - Boost input current
- E_B - Boost input voltage
- E_F - Frequency monitor voltage

The logic diagrams are read from left to right with series blocks indicating "and" conditions and parallel blocks "or" conditions leading to failure indication and transfer.



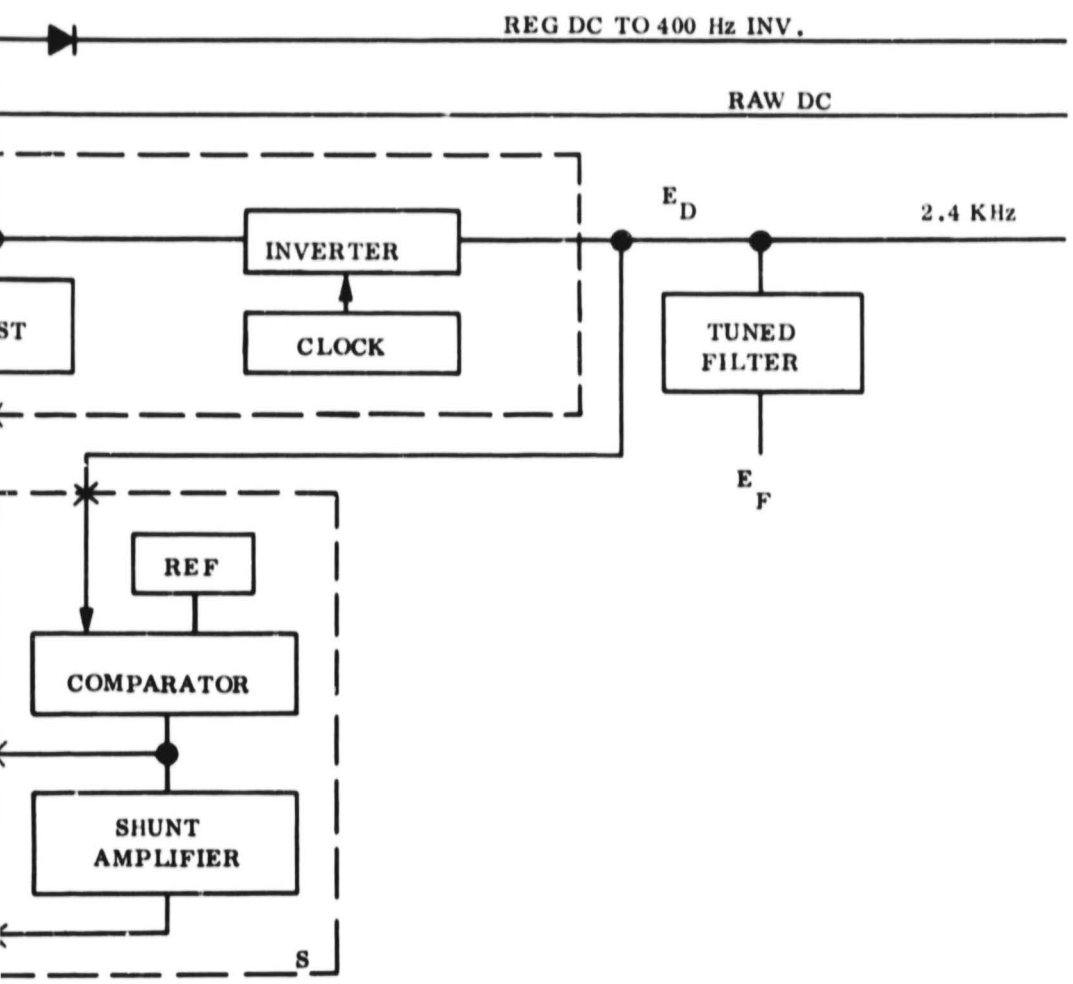
COMPLETE FAULT SENSOR LOGIC

CONDITION NO.				
1	$E_S - KE_D > A$			
2	$E_D > E_{DMAX}$	$E_C < E_{CMAX}$		
3		$E_C > E_{CMAX}$	$I_B > I_{BMIN}$	
4		$E_C > E_{CMED}$		
5	$E_D < E_{DMIN}$	$E_C > E_{CMIN}$		
6		$E_C < E_{CMIN}$	$I_B < I_{BMIN}$	$E_B > E_{BMIN}$
7	$E_F < E_{FMIN}$			

BOOST/INVERTER BLOCK

1 S
DE L

FOLDOUT FRAME 1



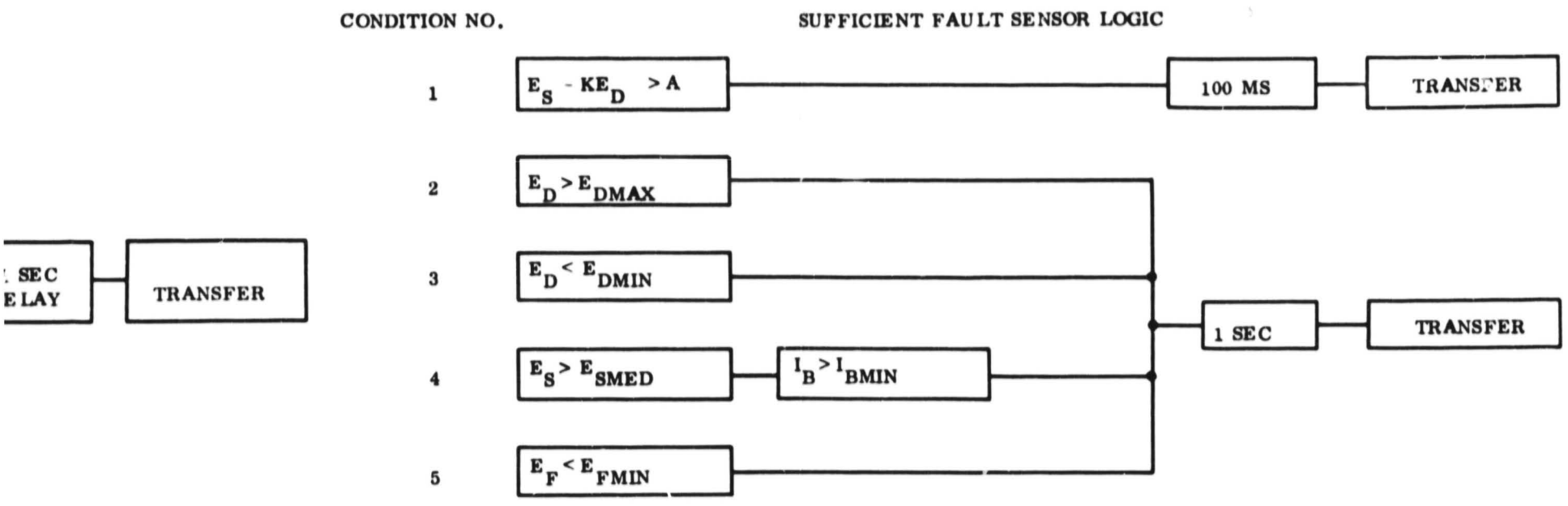


Figure 5.2.6-3. Case III - Boost/Inverter/ Amplifier Groups, Double Block Redundancy

FOLDOUT FRAME 2

The logic distinguishes between internal and external faults. Thus, the over-voltage indication shown in Condition 1 is insufficient reason alone for transfer. If the shunt amplifier voltage does not track the regulated voltage, failure is indicated and transfer initiated. If it does track the output overvoltage (Condition 2) but the boost is operating ($I_B > I_{BMIN}$), failure is also indicated. If this last condition is not fulfilled, the BIA is not at fault and overvoltage may be due to excessive array voltage or insufficient load, both being external fault conditions.

Condition 3 pertains to simultaneous shunt operation (shunting occurs when E_S is higher than some intermediate level designated as E_{SMED}) and boost operation ($I_B > I_{BMIN}$) when under or overvoltage may not be indicated. This is indicative of inefficient system operation due to a possible boost failure or shunt amplifier failure.

Condition 4 is similar to Condition 1, referring to nonproportionality of output and shunt amplifier voltages.

Condition 5 distinguishes whether undervoltage is due to boost failure and absence of battery voltage. If $I_B < I_{BMIN}$, a boost failure may exist. This is corroborated if $E_B > E_{BMIN}$. If $E_B > E_{BMIN}$, the battery has failed. This is a fault external to the BIA and transfer is therefore inhibited.

Condition 6 refers to a clock failure which results in a voltage drop from the tuned filter.

5.2.6.3.2 Sufficient Fault Sensor Definition

This logic eliminates any distinction between internal and external faults for the following reasons:

a. Excess source voltage - This would result from multi-open circuit failures of the array shunt transistors. Since failure of 25 percent of these transistors could be tolerated (see Section 4.6.4.4), there is no expectation of this condition.

b. Insufficient source voltage - This could result from battery failure. If this occurs during battery demand periods, total mission failure is implied, and any need to identify the cause of failure is irrelevant.

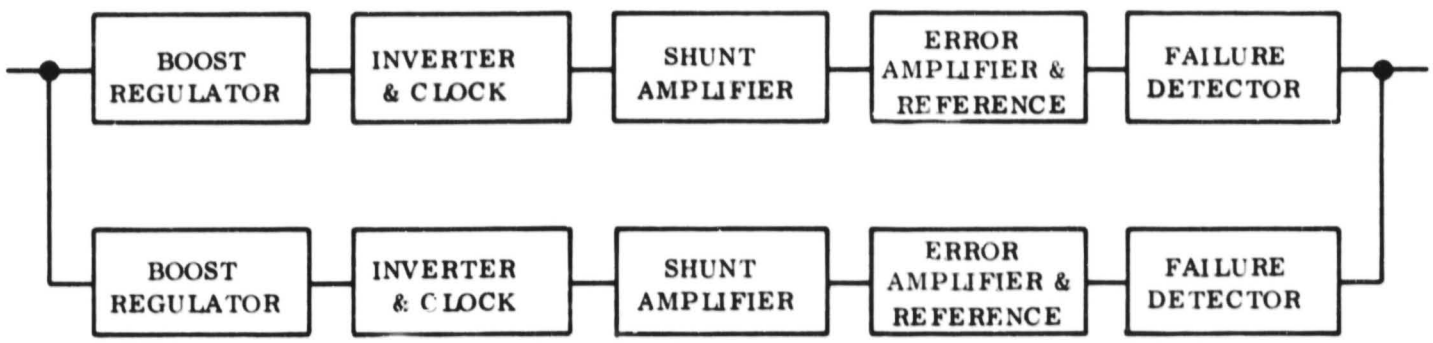
c. Load faults - Loss of critical loads implies mission failure and again any failure identification is irrelevent. Load fault protection for noncritical loads (fuses, circuit breakers) eliminates the necessity for identifying these external faults.

Similar logic diagrams are shown for Cases II and III. Comparing those with Case I, a significant difference lies in the fact that their Sufficient Logic Diagrams are not much simpler than the Complete Logic Diagrams. The reason for this is that with split string redundancy, it is more necessary to distinguish between internal and external faults between blocks since failure in one block appears as an external fault to another block. This distinction must be identified in order to take advantage of split string redundancy in the first place.

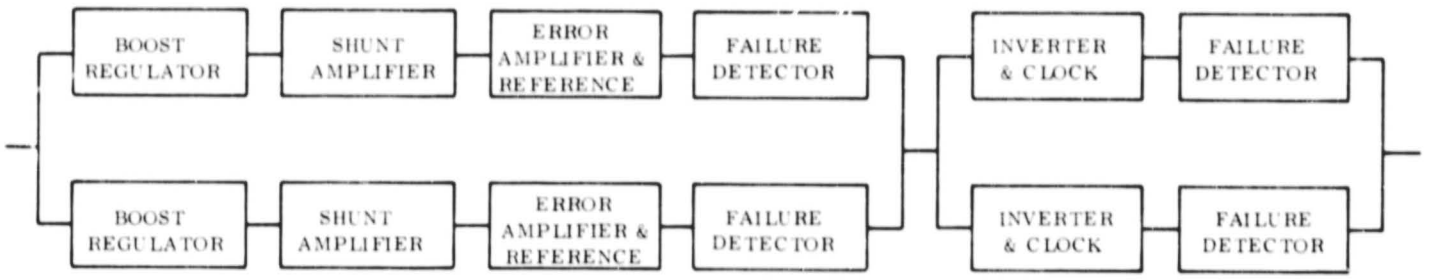
Using the Sufficient Fault Sensor Logic described above, conceptual fault sensor circuits were developed for each case. These were then used in estimating the relative reliabilities described in Section 5.2.7.

Reliability block diagrams for the three cases are shown below:

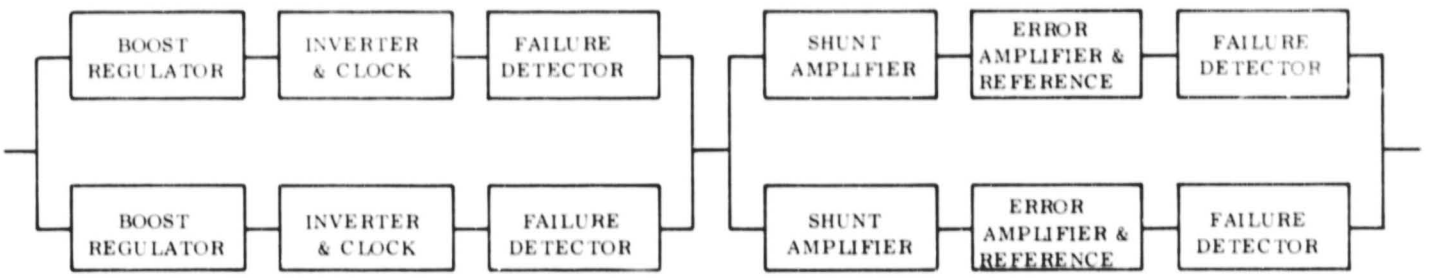
Case I



Case II



Case III



Preliminary circuits were designed and failure rate estimates obtained for each component in each of the three configurations. These failure rates are summarized in Table 5.2.6-1.

Reliability estimates were obtained for each configuration at 1000 hour time increments up to a total of 10,000 hours. The results are plotted in Figure 5.2.6-4.

Table 5.2.6-1. Failure Rate Estimates For Three Redundancy Configurations*

CASE I	%/1000 hrs.
Boost Regulator	0.586
Inverter	0.372
Clock	0.295
Shunt Amplifier	0.090
Error Amplifier and Reference	0.212
Failure Detector	0.961

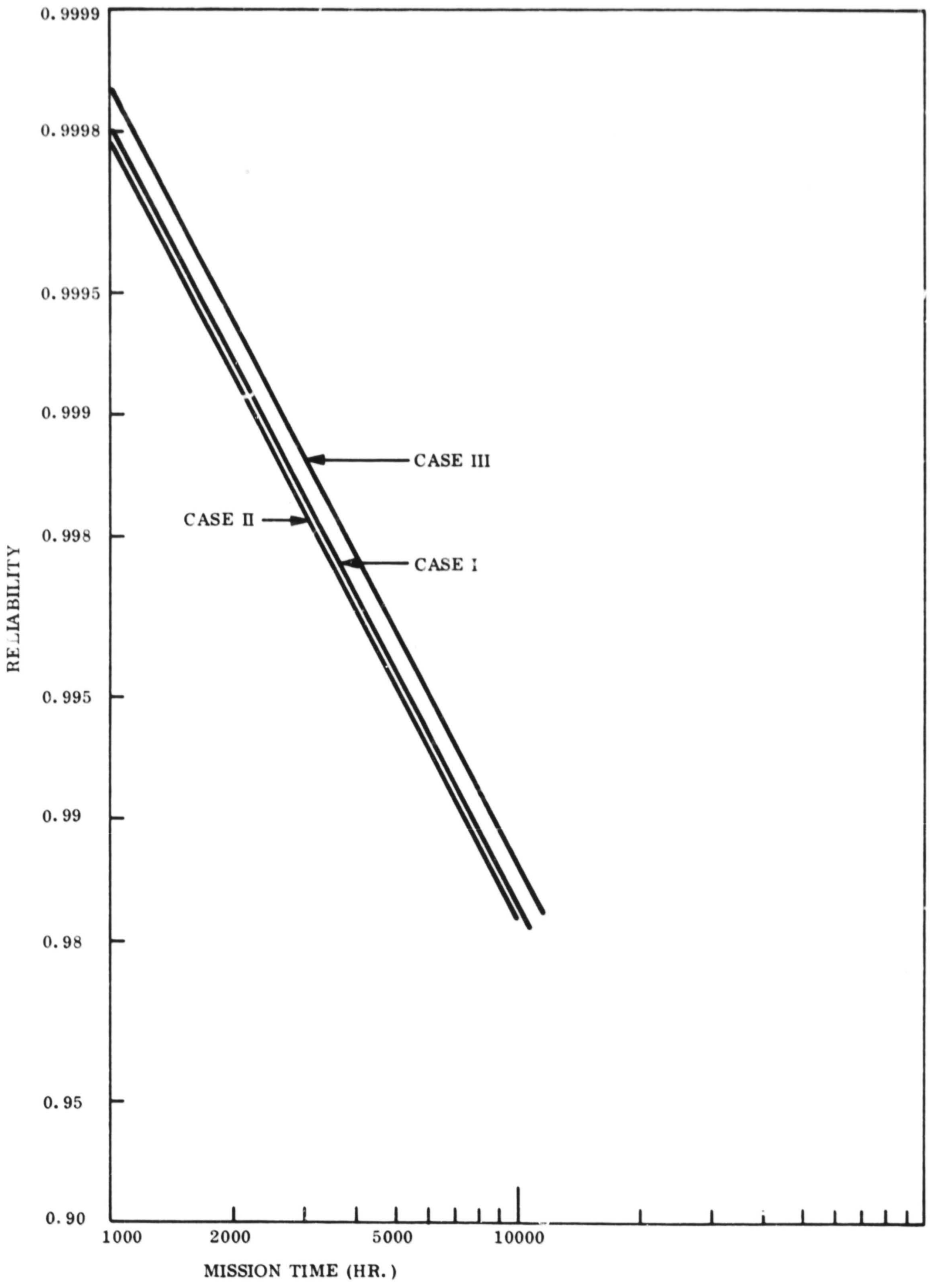


Figure 5.2.6-4. Redundancy Trade Study (BIA)

Table 5.2.6-1. Failure Rate Estimates For Three Redundancy Configurations* (Cont)

CASE II	%/1000 hrs.
Boost Regulator	0.660
Shunt Amplifier	0.090
Error Amplifier and Reference	0.212
Failure Detector	1.290
Inverter	0.372
Clock	0.295
Failure Detector	1.065

CASE III	
Boost Regulator	0.586
Inverter	0.372
Clock	0.295
Failure Detector	0.961
Shunt Amplifier	0.090
Error Amplifier and Reference	0.212
Failure Detector	0.448

*See Section 5.2.10.4

Case III provided the best estimated reliability. Case I was next, and Case II last. The values at the 6500 hour point (approximate orbiter mission time) are given below:

Case III	0.9942
Case I	0.993
Case II	0.9925

It is pointed out that this study was conducted only on the redundant components and the above values are not subsystem reliability estimates. The differences in reliability estimates for three cases was not considered great enough to offset other more positive considerations. Therefore, Case I was selected for the following reasons:

a. Most straightforward and easiest to design due to lowest complexity failure detector (see Guideline, Section 3)

b. Lowest in weight

c. Lowest in cost

d. Least power required for failure detector

5.2.7 REDUNDANT SHUNT SYSTEM RELIABILITY ESTIMATE

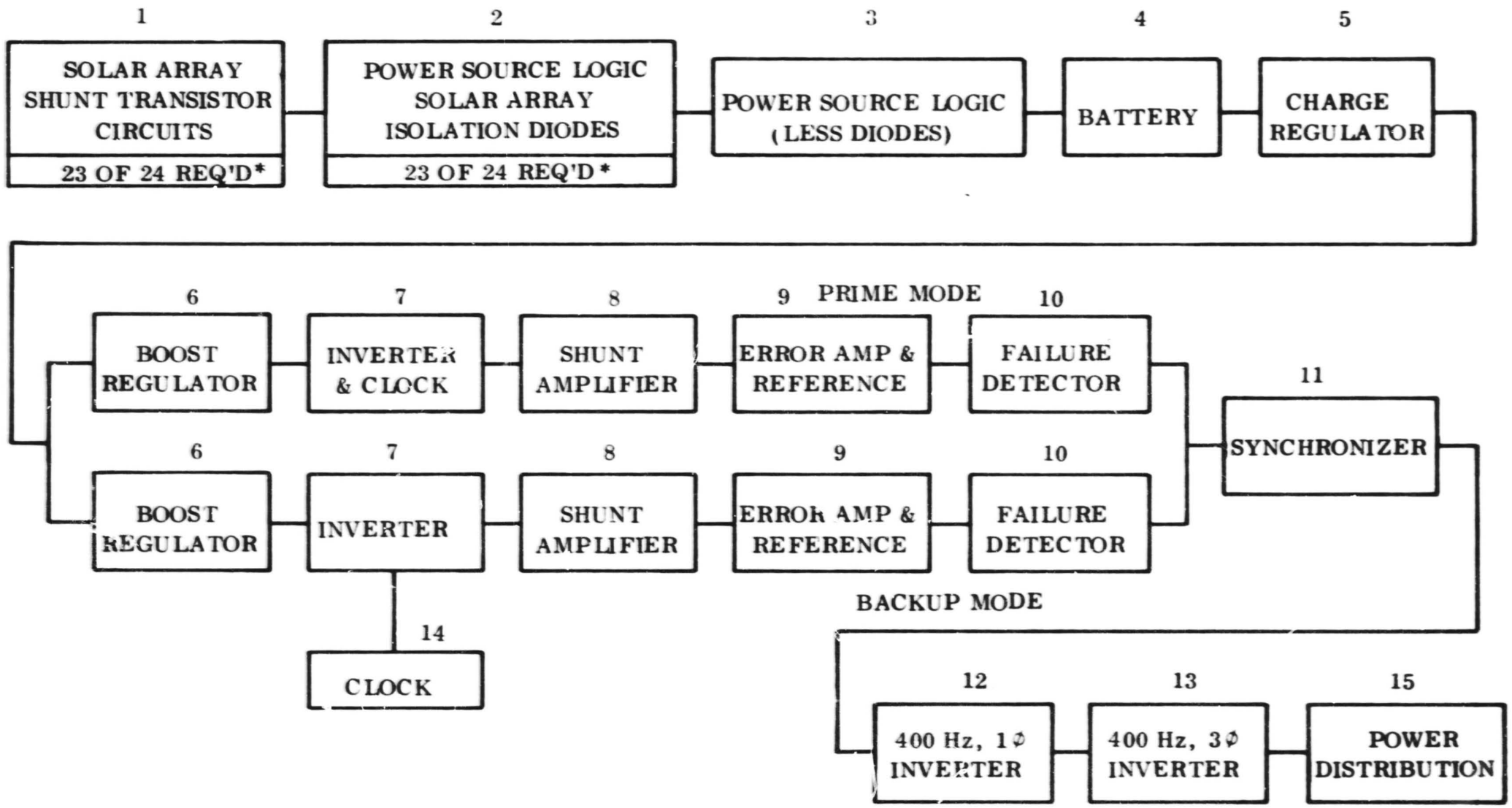
A subsystem reliability estimate was computed using the selected Case I redundancy configuration as discussed in Section 5.2.6.

5.2.7.1 Reliability Block Diagram

The reliability block diagram for this configuration is given in Figure 5.2.7-1. The assumptions given for the single string shunt system in Section 5.2.5.1 also apply here with the following exception and addition:

a. In the event of an inverter clock failure when the subsystem is operating in the prime mode, the subsystem will switch to the backup mode. If there is an inverter clock failure when the subsystem is operating in the backup mode, degraded performance will result due to loss of frequency accuracy.

b. The failure detector has been split into two sections. The portion assigned to the prime mode represents those items which, if they fail, would cause the subsystem to switch to the backup mode. The portion assigned to the backup mode represents those items whose failure would make it impossible to switch to the backup mode if a failure occurred in the prime units.



* ALLOWABLE FAILURE OF SHUNT TRANSISTOR CIRCUIT AND ISOLATION DIODE ARE MUTUALLY EXCLUSIVE EXCEPT WHEN BOTH ARE ON SAME ARRAY SECTION.

Figure 5.2.7-1. Mariner Power Subsystem Redundant Shunt System Reliability Block Diagram

5.2.7.2 Mission Profile

The assumed orbiter mission profile given in Section 5.2.3.2 was used for this analysis.

5.2.7.3 Hardware Failure Rates

The failure rates used for this configuration are given in Table 5.2.5-1. The assumptions relative to failure rates and stress level multipliers in Section 5.2.3.3 also apply here.

5.2.7.4 Sensitivity Studies

The areas most sensitive to additional reliability improvement were identified by individually reducing component failure rates by a factor of 10 and computing subsystem reliability as performed for the Mariner '69 Redundant Power Subsystem. The results are plotted in histogram form in Figure 5.2.7-2.

5.2.7.5 Results

A review of Figure 5.2.7-2 indicates that additional reliability improvement can be obtained by improving the power distribution, the battery, and the Power Source Logic. The limitations on additional effort in these areas have been discussed in Section 5.2.4.5. (Note leveling of all elements except the power distribution and the battery). As pointed out in Section 5.2.1.2.1, further system improvement should be sought by working on the least reliable elements.

The resulting probabilities of good, degraded, and failed modes for the final shunt system are as follows:

Probability of no subsystem failure	= 0.8628
Probability of Degraded Mode 1 (clock failure)	= 0.0008
Probability of Degraded Mode 2 (1 battery cell shorted)	= 0.0697
Probability of Mission Failure	= 0.0668

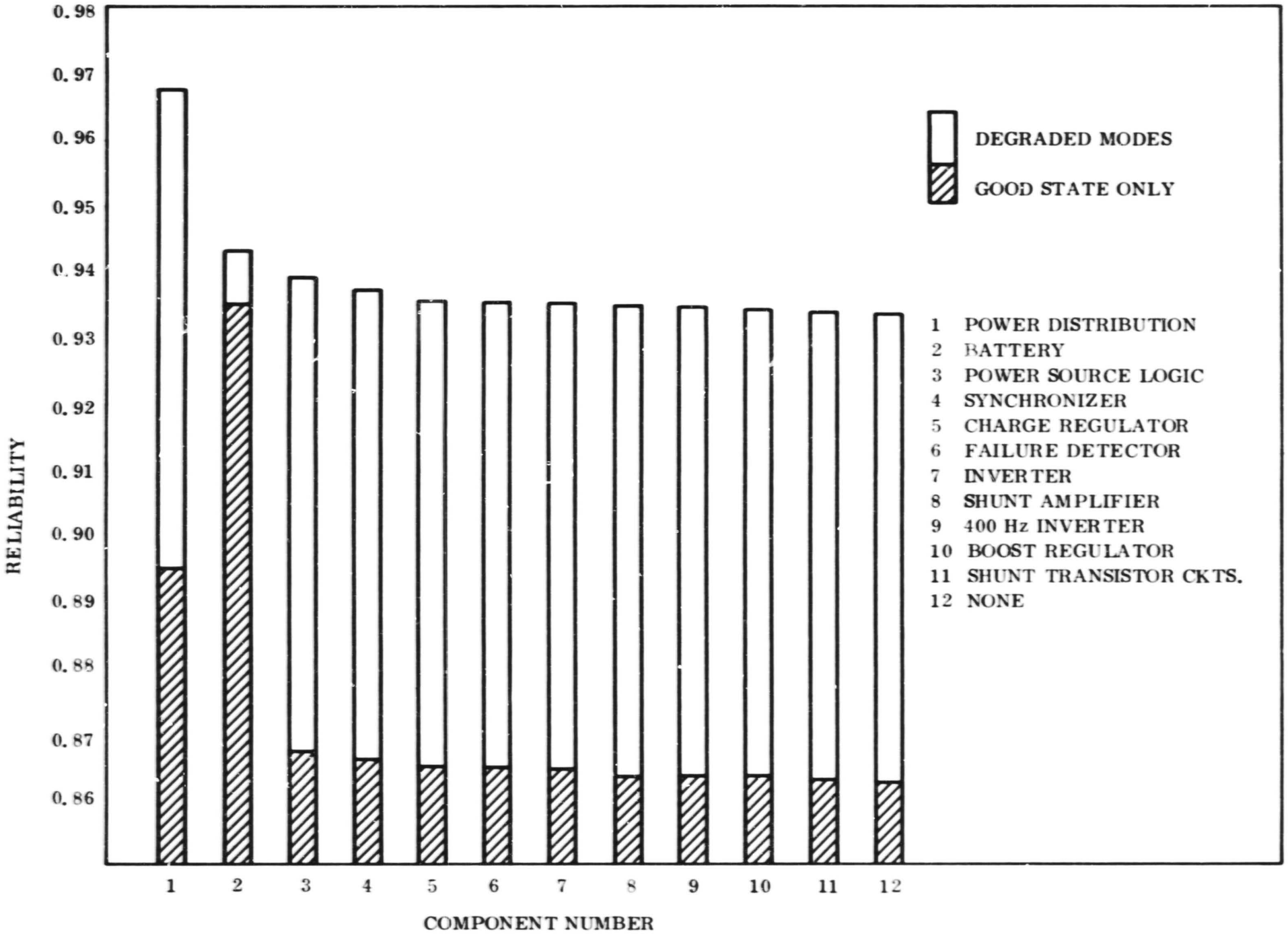


Figure 5.2.7-2. Reliability Resulting From 10 To 1 Improvement In Failure Rate Of Indicated Component - Shunt Regulator Power Subsystem

5.2.8 COMPARATIVE RESULTS

The estimated power subsystem reliability for each of the configurations discussed in the preceeding paragraphs are summarized as follows:

Configuration	Probability of Good State	Probability of Good and Degraded States
MM'69 Single String	0.7766	0.8556
Shunt System Single String	0.8163	0.8994
MM'69 Redundant	0.8305	0.8984
Shunt System Redundant	0.8626	0.9332

The above figures are the estimated power subsystem reliability values for the orbiter mission (6516.7 hours). The fact that the shunt system figures are better, is the result of a concerted effort to improve reliability throughout all phases of the study. The areas which require further investigation are the power distribution section and the battery. Also a failure mode and effect analysis down to the piece part level should be performed during the detailed design phase to preserve the inherent subsystem reliability.

5.2.9 OTHER CONSIDERATIONS

5.2.9.1 Reliability/Weight Optimization

The previous cases discuss the baseline reference system (MM'69/orbiter profile) and the final selected version of the shunt system. During the study, many minor and major variations were evaluated. Table 5.2.9-1 lists the specifics of several important variations studied in detail and gives the calculated probabilities of success for each, along with the estimated subsystem weight. The reason for the small subsystem weight differences can be seen by examining Figure 5.2.9-1 which shows the relative weights of the power system functional modules. Examination of these weights indicates that the total power system weight is dominated by the array and battery. The weights of the remaining eight modules are sufficiently small (on a system basis) to allow the system to be optimized from a reliability standpoint without regard to these weights.

Table 5.2.9-1. Reliability Comparative Studies

Case No.	Case Description	Probability of Complete Success	Probability of Success in Degraded Mode**	Weight (Pounds)	
				Subsystem Less Array & Battery	Total Subsystem
	Shunt System: Boost/Inverter/Reference-Error Amplifier all block redundant - Case I and;				
A	• Boost on full mission* • Synchronizer on full mission • Charge Regulator and Shunt Amplifier & Transistors always on except during launch • 3Ø, 400 Hz Inverter on during cruise and when required	0.8184	0.8856	40.03	120.83
B	• Same as A except: Synchronizer and charge regulator are redundant	0.8666	0.9377	41.83	121.83
C	• Boost on full mission • Synchronizer, 400 Hz-3Ø Inverter, and charge regulator only on when required • Shunt Amplifier and transistors always on except during launch	0.8603	0.9309	40.03	120.83
D	• Same as C except: Boost on only when required Shunt Amplifier & transistors only on when required	0.8626	0.9332	40.03	120.83

* On & Off in this table refer to operating hours used in computing reliability

** Degraded mode as defined in Section 5.2.7.5

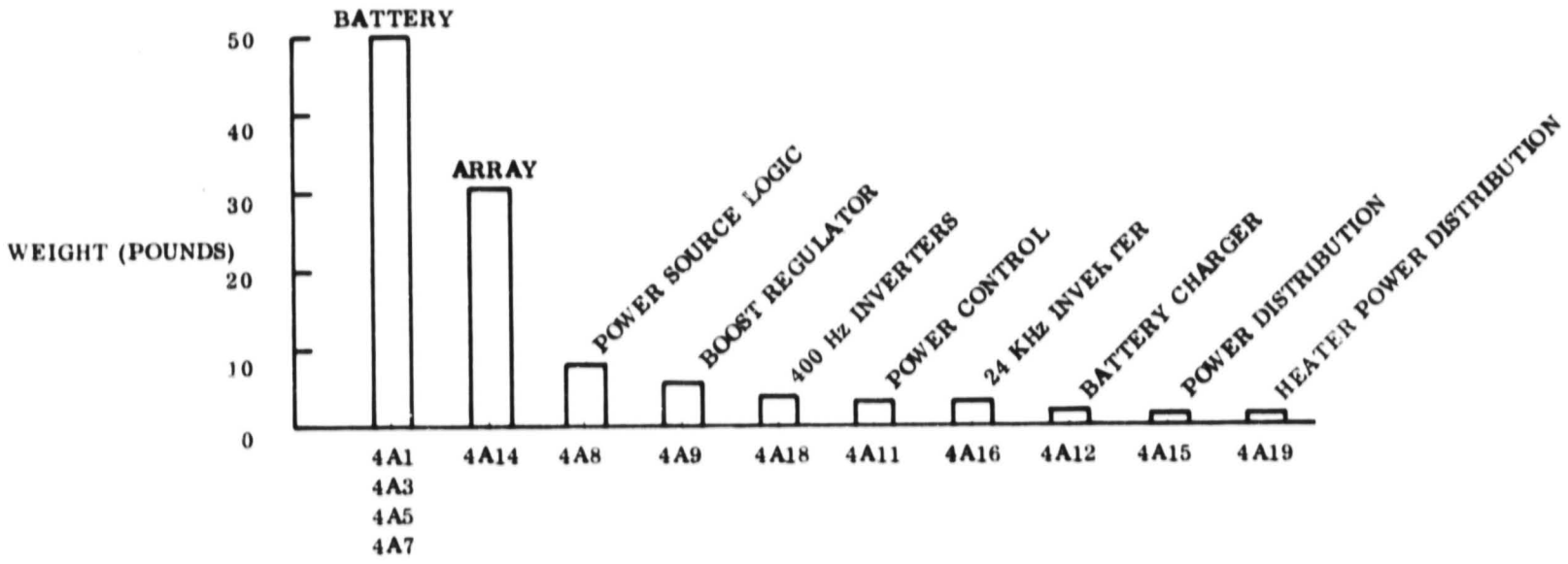


Figure 5.2.9-1. Single String Weights

5.2.9.2 Piece Part Versus Black Box Redundancy Approach

Redundancy is generally used to improve system reliability beyond the level achievable through other means which are directed towards improving the reliability of equipment, parts, or materials. It is well known that redundancy indicates higher reliability when applied at lower levels, assuming that no additional complexity is required. That is, the computed reliability for a completely duplicated system will be less than that for a system whose components are individually redundant, again assuming no additional complexity is required for the latter case. Theoretically, individual piece part redundancy should provide the best reliability if the assumption of no additional complexity and independence of failure is made. In practice, however, there are several severe restrictions to complete application of piece part redundancy. Some of the more obvious ones are:

a. Some devices such as transformers and zener diodes will not function normally in a paralleled configuration.

b. Generally, independence of failures cannot be maintained, i.e., the failure of one device will have some effect on the performance of the remaining good device or devices.

c. Testing to assure that all elements are working is difficult and sometimes impossible.

d. Reasons a, b, and c make it difficult to implement Guideline 3.6 (Section 3).

One of the most serious disadvantages to use of piece part redundancy is the introduction of additional single failure points. These vary in complexity from the junctions of several redundant parts to complex interaction effects resulting from degradation of one of the redundant parts. The latter effect would require thorough evaluation and could present serious design problems.

In power systems the use of black box redundancy generally requires failure detection and switching. The redundant element, however, can be operated on a standby basis and overall efficiency is usually better and the weight penalty is minimal.

The black box redundancy approach has been selected as the most practical approach during this Phase I system level study. It is anticipated that additional system reliability improvement can be achieved at the circuit level by the use of selected piece part redundancy, during a Phase II detail design activity. For example, three specific cases of piece part redundancy which should be studied are:

a. The use of two transistors in series for the shunt regulator dissipators discussed in Section 4.4.4

b. The use of two transistors in series for dissipative regulators, e.g., battery charger and other series dissipative regulators in failure detector, in boost regulator, and in 2.4 kHz inverter

c. The use of a redundant Earth-Mars mode switch

5.2.10 SUPPORTING DATA

5.2.10.1 Summary of Functional Element Failure Rate Estimates

The parts count and estimated faulure rates for each functional element using both GE and MIL-HDBK-217A part failure rates are given in Table 5.2.10-1 for MM'69. The MIL-HDBK-217A rates were used for all reliability computations.

5.2.10.2 Nonoperating Failure Rates

The ratio of operating to nonoperating failure rates was obtained from a review of RADC Report RADC-TR-66-348. "Dormant and Storage Effects on Electronic Equipment and Part Reliability". The results used are summarized in Table 5.2.10-2.

The ratios of operating to nonoperating failure rates range from 2 to 200 for various types of parts. Although the ratios for most of the high usage parts are above 10, this conservative value was selected because the standby units are not dormant in the same sense as shelf life units and most of the data in the RADC report was based on parts in storage conditions. Many of the standby units in the power subsystem will have voltage applied to some parts, although no current is being conducted.

5.2.10.3 Calculation of False Switching Failure Rates

A preliminary reliability analysis was performed on the JPL and GE failure detector designs to estimate the false switching failure rate as required for use in the standby redundancy model. These estimates are based on failure effect analyses which categorize the effect of individual part failures as resulting in false transfer, no transfer, or no effect.

Part failure rates were assigned an exponential failure density model. This was assumed to compute the total failure rate and the false switching failure rate for each failure detector (see Table 5.2.10-3 and 5.2.10-4). The part failure rates were obtained from the table of Minimum Part Class and Type Failure Rates in MIL-HDBK-217A in accordance

Table 5.2.10-1. Power System Parts Count And Failure Rates

Part Type	Failure Rates (%/1000 hrs) GE	Failure Rates (%/1000 hrs) MIL-HDBK-217A	Power Source Logic* 4A8	Boost Regulator 4A9 4A10	Power Control 4A11	Battery Charger 4A12	Power Distribution 4A15	Inverter 4A16 4A17	Free Run 4A16 4A17	Clock 4A16 4A17	400 Hz, 3Ø Inverter 4A18	400 Hz, 1Ø Inverter 4A18	Synchronizer 4A18	Power Distribution 4A19
XTAL	0.002	0.002								1				
Resistors - Film	0.00025	0.007	33	24	21	9	46	1	3	15	12	6	3	11
" - Composition	0.00025	0.00035	3	5	17	22	1	5			3	2		
" - Wirewound	0.02	0.0006	2	3	1	9		4		1	6	4	2	
" - Variable	0.02	0.088		2										
Capacitors - Teflon	0.0007	0.0001			1									
" - Ceramic	0.0006	0.0002											2	
" - Glass	0.0006	0.00014	1							6				
" - Mica	0.012	0.00003												
" - Paper	0.0007	0.00001		2		2		1			1	1		
" - Tantalum Foil	0.036	0.0043	2	7		6	9							
" - Tantalum Solid	0.01	0.0005	12	4	11	2	12	1		4	1	1	2	5
SCR	0.0015	0.02		2										
Diodes	0.0005	0.01	29	11	17	11	42	2		7			13	9
Zener Diodes	0.0385	0.03	5	2	8	3	1			3				
Transistors	0.001	0.01	2	9	7	13	5	4		4	9	5	2	1
Transformers	0.04	0.02	7	4	6	2		2	1	1	4	2	1	2
Magnetic Amplifiers	0.02	0.02	7											
Inductors	0.02	0.02	1	1				1			1	1		
Fuses	0.01	0.01	5		2	**								*** 1
Switches	0.08	0.002	1											
Connectors	0.01	0.001	6	1	2	1	2	1			1	1		2
Relays	0.001	0.00002			2	3	3							1
Integrated Circuits	0.005	0.005								7			3	
TOTAL (GE)			1.0806	0.68515	0.7457	0.65215	0.54325	0.2072	0.04075	0.26735	0.33345	0.2077	0.12545	0.16925
TOTAL (MIL-HDBK-217A)			1.07679	0.78067	0.78119	0.47398	0.86911	0.13266	0.041	0.36544	0.280	0.1566	0.2086	0.23152

* Power Source Logic parts count does not include solar array isolation diodes.
** Two Paralleled Fuses
*** Also 13 sets of two paralleled fuses.

Table 5.2.10-2. Comparison of Operating Versus Non-Operating Failure Rates

Part Type	Failure Rate (%/1000 hrs) Operating	Non-operating	Ratio(minimum)
Resistors, Film	0.01	0.0001	100
" , Composition	0.02	0.0005	40
" , Wirewound	0.001	0.00001	100
" , Variable	0.02	0.001	20
Capacitors, Glass	0.001	0.00001	100
" , Paper	0.01	0.00005	200
" , Tantalum	0.02	0.0005	40
Diodes, Hi Power	0.2	0.02	10
" , Med Power	0.002	0.001	2
" , Low Power	0.005	0.0005	10
Transistors, Hi Power	0.05	0.05/0.005	10
" , Med Power	0.1	0.002/0.005	20
" , Low Power	0.01	0.001	10
Transformers, Power	0.0005	0.0001	5
" , Pulse	0.001	0.00005	20
Inductors, Power	0.005	0.0005	10

with the "Reliability Ground Rules" in the EOS Design Review Report. The assumed subdivision of the part failure rates into "open" and "short" failure rates is shown in Tables 5.2.10-3 and 5.2.10-4.

The total failure rate estimate for the MM'69 failure detector did not agree with the value shown in the EOS Design Review Report. It was noted that three variable resistors contributed approximately half of the total estimated failure rate, which reflects the high figure for these resistors given in MIL-HDBK-217A. The specific value used by EOS is not given in the Design Review Report. The false switching failure rate was

Table 5.2.10-3. GE Failure Detector Computation of False Switching Failure Rate Estimate

Part Type	Total		False Switching Due To:			
			Open		Short	
	Qty.	Failure Rate*	Qty.	Failure Rate*	Qty.	Failure Rate*
Resistors, Film	40	0.007	15	0.007	--	--
Resistors, Wirewound	1	0.0006	--	--	--	--
Capacitors, Mica	3	0.00003	--	--	1	0.00002
Capacitors, Tantalum	18	0.0005	1	0.0001	5	0.0004
Diodes	39	0.01	6	0.002	10	0.008
Transistors	6	0.01	--	--	4	0.008
Transformers	4	0.02	--	--	4	0.01
Integraged Circuits	10	0.005	4	0.002	2	0.003
TOTALS		0.86969		0.1251		0.16002

False Switching Failure Rate = 0.1251 + 0.16002 = 0.28512

Ratio of False Switching to Failure Rate = $\frac{0.28512}{0.86969}$ = 0.33

* All Failure Rates are in %/1000 Hrs.

Table 5.2.10-4. MM'69 Failure Detector Computation of False Switching Failure Rate Estimate

Part Type	Total		False Switching Due To:			
			Open		Short	
	Qty.	Failure Rate*	Qty.	Failure Rate*	Qty.	Failure Rate*
Resistors, Film	11	0.007	5	0.007	--	--
Resistors, Composition	10	0.00035	5	0.00035	--	--
Resistors, Variable	3	0.088	3	0.088	--	--
Capacitors, Tantalum	7	0.0005	1	0.0001	3	0.0004
Diodes	11	0.01	1	0.002	7	0.008
Transistors	7	0.01	--	--	7	0.008
Transformers	1	0.02	1	0.01	1	0.01
TOTALS		0.5480		0.31285		0.1232

False Switching Failure Rate = 0.31285 + 0.1232 = 0.43605

EOS Failure Detector Failure Rate ** = 0.293

Ratio of False Switching to Total Failure Rate, with Variable Resistors = $\frac{0.43605}{0.548} \approx 0.8$

Ratio of False Switching to Total Failure Rate, without Variable Resistors = $\frac{0.17205}{0.284} \approx 0.6$

Average Ratio = 0.7

Equivalent False Switching Failure Rate = 0.7 x 0.293 = 0.2051

* All Failure Rates are in %/1000 Hrs.

** From EOS Design Review Report, 7178-DRR-002A, 4/17/67

therefore obtained by taking the average of the ratios of estimated false switching rate to total failure rate, including and excluding the variable resistors, and then multiplying the EOS failure detector failure rate by this average ratio.

The results for both the MM'69 and GE failure detectors are as follows:

	Failure Rate (%/1000 hrs.)	
	False Switching	Total
GE	0.285	0.870
MM'69	0.436	0.548
MM'69 Modified	0.205	0.293

5.2.10.4 Trade Study Failure Rates

The shunt system trade study was performed on three redundant configurations of the Boost Regulator (B), Inverter (I), and Shunt Amplifier Section (including the Error Amplifier and Reference) (A), as shown in Section 5.2.6. As discussed in Section 5.2.6, each configuration requires different failure detector sensors and logic. In addition a current overload monitor is required for the inverter, and a modification to the boost regulator is required for Case II.

The failure detector failure rates for each case were obtained by applying MIL-HDBK-217A part failure rates to part quantities obtained from preliminary circuit designs. These are summarized in Table 5.2.10-5.

The estimated failure rates for the inverter and booster modifications shown in the table were modified as follows to normalize the results for compatibility with the existing failure rate estimates:

Table 5.2.10 5. Trade Study - Failure Rates

Part Type	NUK-HDBK-217A Fail. Rate (%/1000 Hrs.)	Quantity of Each Part								
		Shunt Ampl.	Error Amp. & Ref.	Inverter Overload Monitor	Case II Boost Reg. Add.	Case I Fail. Det.	Case II Fail. Det. (I)	Case II Fail. Det. (B, A)	Case III Fail. Det. (A)	Case III Fail. Det. (B, I)
Resistor, w.w.	.0006	1				1	1	1	1	1
Resistor, Film	.007	7	12	7	4	39	40	36	20	39
Resistor, Variable	.088		1			4	5	7		4
Diode	.01			1	5	9	16	15	5	9
Zener Diode	.03		1	1		2	2	1		2
Transistor	.01	4	1			10	8	5	4	10
Capacitor	.0005	1			1	11	9	13	1	11
Transformer	.02			1	1	4	2	8		4
Magnetic Amp.	.02			2						
Integrated Ckts.	.005							5	1	
TOTAL FAILURE RATE (%/1000 HRS)		0.090	0.212	0.149	0.0985	0.961	1.065	1.290	0.236	0.961

a. Inverter

- o Estimated failure rate for inverter (including free run) using MIL-HDBK-217A failure rates (from Table 5.2.10-1) = 0.17366 %/1000 hrs
- o Additional failure rate for current overload monitor (from Table 5.2.10-5) = 0.149 %/1000 hrs
- o Existing failure rate from EOS Design Review Report = 0.200 %/1000 hrs
- o Normalized Value:

$$\frac{0.17366 + 0.149}{0.17366} \times 0.200 = 0.372 \text{ \%/1000 hrs}$$

b. Boost Regulator

- o Estimated failure rate for the boost regulator using MIL-HDBK-217A failure rates (from Table 5.2.10-1) = 0.78067 %/1000 hrs
- o Addition failure rate (from Table 5.2.10-5) = 0.0985 %/1000 hrs
- o Existing failure rate from EOS Design Review Report = 0.586 %/1000 hrs
- o Normalized Value:

$$\frac{0.78067 + 0.0985}{0.78067} \times 0.586 = 0.660 \text{ \%/1000 hrs}$$

5.3 EQUIPMENT DESIGN STUDIES

5.3.1 SHUNT EQUIPMENT STUDIES

With the proposed method of mounting the shunt transistors on the solar array, several environmental factors were of concern:

- Effect of large temperature variations on electrical performance and mechanical integrity
- Effect of the ionizing radiation environment on the shunt transistor characteristics

Special studies of these factors were conducted and are described below.

5.3.1.1 Low Temperature Power Transistor Characteristics

Tests have been made of some of the parameters of power transistors at very low temperatures to evaluate the feasibility of locating these devices on the solar array. Solitron Devices Incorporated recommended type 8071 for this application and loaned eight 8071 and two 8070 transistors for the purposes of the test.

The results indicate that these power transistors will have sufficient gain to function effectively at the lowest temperatures that are expected to reach.

5.3.1.1.1 Test Description

The eight transistors were tested in two groups of four each. Preliminary tests were conducted with standard voltmeters and ammeters to establish voltage and current ranges. A multichannel data recording instrument (Hewlett-Packard Data Acquisition System Model 2010C) was connected to obtain accurate data. Measurements were made at approximately 0.25, 0.5, 1.0, 2.0 and 5.0 amperes for each transistor. Time, temperature, base current, collector current, base voltage and collector voltage were recorded for every point. The use of the recording instrument made is possible to obtain highly accurate characteristics of the four transistors (20 point measurements) in approximately 90 seconds. Speed was required to obtain essentially isothermal data.

In addition to the above measurements, the second group of transistors (two 8070's and two 8071's) were cycled 20-times between +200°F and -200°F in the de-energized condition.

5.3.1.1.2 Equipment

The tests were conducted in a chamber normally used for space environment thermal vacuum cycling. Since the normal thermal control consisted of limit switches only, the base plate temperature was manually regulated. Procedure consisted of driving the base plate temperature to the lowest value desired and then allowing the temperature to rise slowly toward room ambient. The temperature of the heat sink was automatically sensed and recorded for each measurement with an accuracy of ±0.25°F.

The transistor heat sink consisted of a copper plate with dimensions of 6 by 6 by 1/2 inches. The heat sink was bolted to an 8 inch diameter copper base plate with a 1 inch thickness. The base plate contained channels for liquid nitrogen cooling and resistive elements for heating. The transistors were mounted directly to the heat sink by means of drilled tapped holes to provide maximum thermal contact. Silicon grease was used at all interfaces. The transistors were mounted in a square configuration approximately 2.3 inches between centers on a side. Thermocouples were placed on the base plate, on the edge of the heatsink and at the center of the square array of transistors. The latter thermocouple was 1.6 inches from each transistor and provided the measurements recorded in the tests. All three thermocouples were monitored during the tests. The thermocouple at the edge of the heat sink showed no measurable difference in temperature from the thermocouple at the center of the heatsink. The baseplate thermocouple showed temperature differences of 10°F to 15°F when liquid nitrogen was flowing or the heater was operating. When the temperature control elements were inactive and the system was allowed to reach steady state, all three thermocouples indicated the same temperature within the accuracy of the monitoring equipment (±2°). When the steady state condition was reached, the central thermocouple was switched from the monitoring equipment to the recording system and the thermocouple voltage was read directly. The temperature was then accurately deduced from thermocouple tables.

The chamber was cubical with a 12 inch dimension on each side. A window was included for observation. A vacuum was maintained at all times to eliminate the possibility of condensation.

All instruments used including the automatic data recording system were properly in calibration and were carefully rechecked before and after the tests to ensure the validity of the data.

5.3.1.1.3 Measurement Evaluation

The results of the measurements show that all the selected power transistors have usable gain at lowest temperature which is expected to be encountered (-200°F). Furthermore, there is no indication of rapid gain deterioration below this temperature. If it is assumed that the eight samples tested are typical, it is not unreasonable to consider applications at temperatures as low as -300°F.

Representative measurements for each transistor are presented in Figures 5.3.1-1, 5.3.1-2 and 5.3.1-3. Since temperature control was not available, the environment chamber was cooled to temperatures in the vicinity of -300°F and then allowed to drift upward. The temperature variation during the runs plotted was approximately 2°F. The temperature at the beginning and end of each run is shown with each curve.

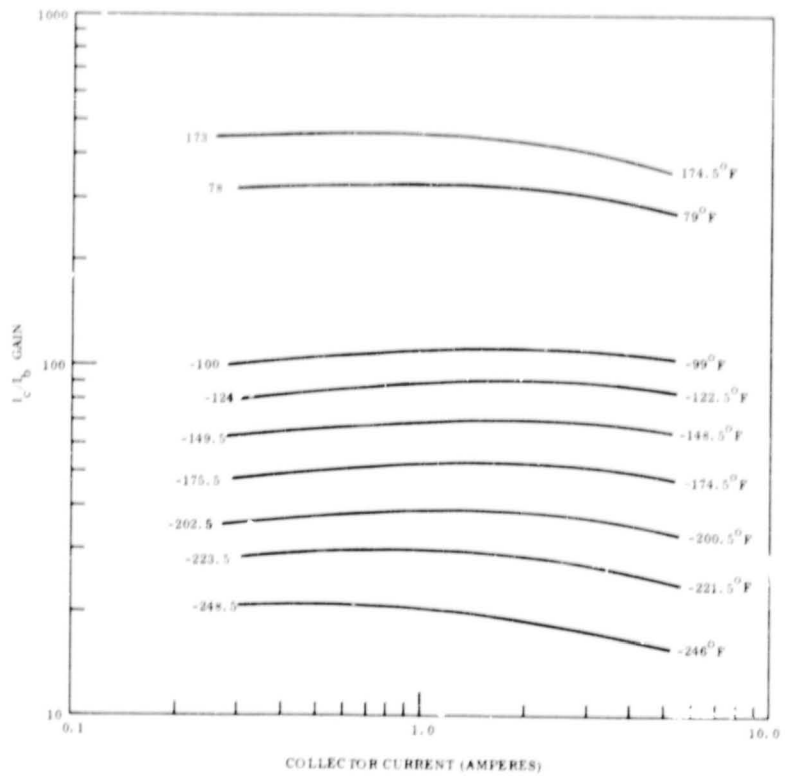


Figure 5.3.1-1. Transistor Gain Versus Collector Current (Type 8071)

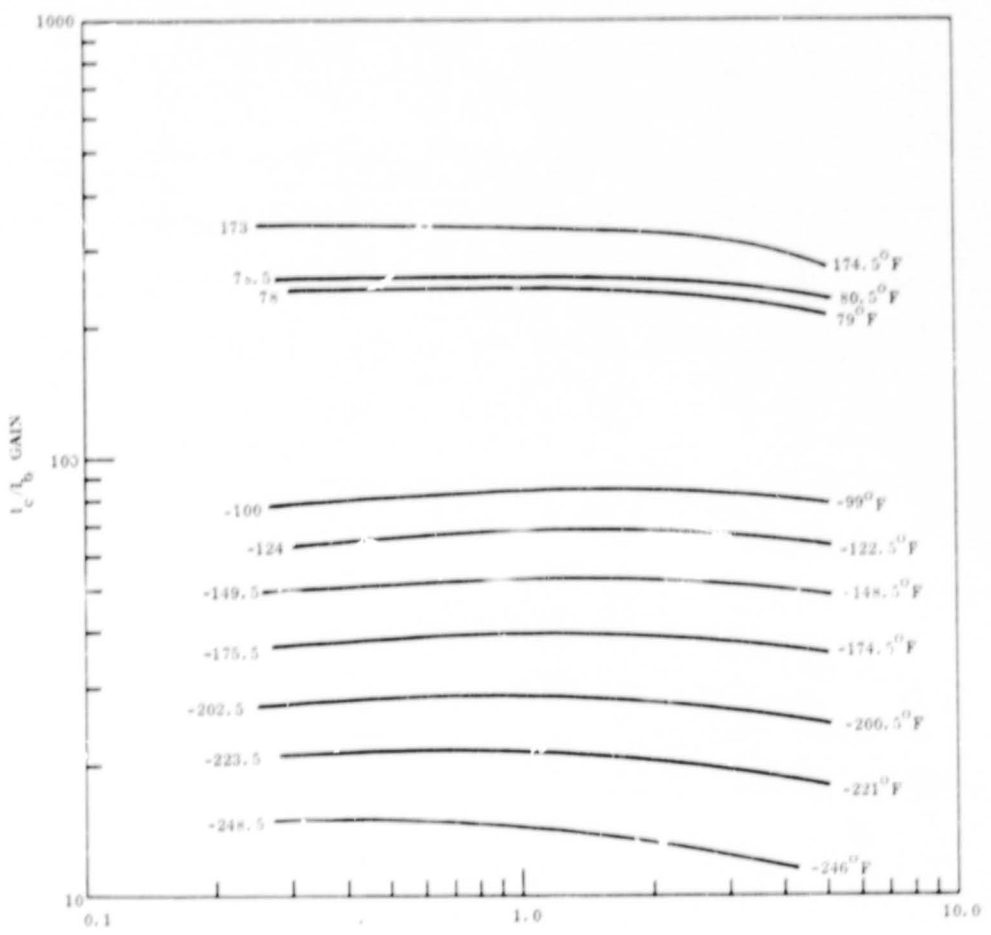


Figure 5.3.1-2. Transistor Gain Versus Collector Current (Type 8070)

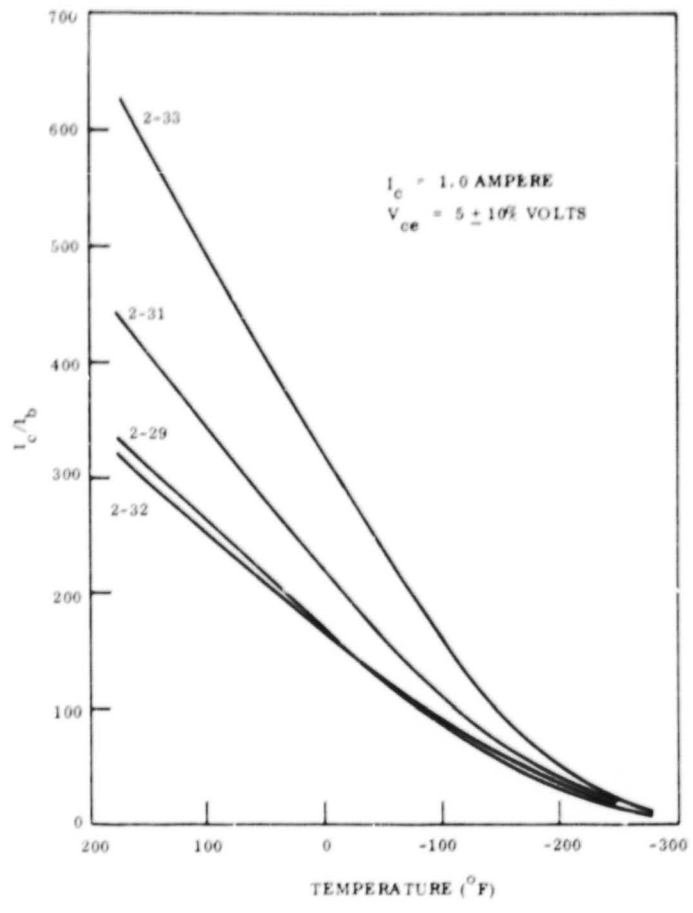


Figure 5.3.1-3. Gain Versus Temperature (Type 8070 and 8071)

The gains of the second group were checked at room ambient (+80°F) after the initial test cycle. The result is illustrated in Figure 5.3.1-2. A consistent decrease in gain was measured on all four transistors. Allowing for a slight temperature difference between the two measurements, the discrepancy is approximately -5 percent. Since the measurement accuracy of the test equipment is at least three significant figures, it was concluded that a gain change had taken place. This observation instigated further testing and the second group of transistors was subjected to 20 temperature cycles from +200°F to -200°F with approximately 90 minutes for each cycle. The transistors were not energized during these tests. No further gain deterioration was observed.

A comparison of transistor gain at 1.0 ampere over the full range of temperatures used in the tests is illustrated in Figures 5.3.1-3. These figures show that it cannot be assumed that the transistors which have the highest gain at high temperatures will have the highest gain at low temperatures. Further, transistors intended for low temperature applications cannot be selected on the basis of gain alone at higher temperatures. However, on the basis of the eight transistors measured, it appears reasonable that a selection may be made on the basis of gain and the rate at which gain decreases with temperature at higher temperatures. Some measured values of gain at one ampere are provided in the following table.

Transistor	2-32	2-33	2-31	2-29	1-32	1-33	1-31	1-29		Residual
Type	8070	8071	8071	8070	8071	8071	8071	8071	$\bar{G}$	%
80°F	236	455	323	241	495	194	243	406	324	100
-200°F	30.8	47.1	38.4	28.6	36.3	25.7	31.3	45.6	35.5	11
-280°F	7.99	9.42	10.0	7.10	9.05	7.52	8.76	11.7	8.94	2.76

These plots also indicate a higher degree of gain stability with temperature and current for the lower gain transistors. Selection of transistors for a specified circuit would depend on the relative critical aspects of gain stability and the magnitude of gain in that application.

Saturation resistance measurements were made by adjusting the collector current to 5.0 amperes. The collector voltage was then reduced until the collector current decreased to 2.5 amperes. Measurements made at these points indicate no significant changes in saturation resistance, although in general the value decreased with decreasing temperature. Base voltage measurements increased with decreasing temperature but remained within specification at -200°F.

5.3.1.1.4 Summary

a. The transistors tested showed no physical damage from exposure to a low temperature of -300°F. Twenty temperature cycles between +200°F and -200°F produced no significant change in characteristics measured at 80°F.

b. At -200°F the transistors retain approximately 10% of the gain measured at 80°F. For the transistors tested, $H_{FE}(-200^{\circ}F) > 20$. This represents more than adequate gain for most power transistor applications.

c. Saturation resistance and base voltage characteristics remained within specification at -200°F.

d. There was no indication at any point in the experiment that operation at temperatures in the vicinity of -200°F offered any critical problems.

5.3.1.2 Shunt Transistor Radiation Effects

An assessment of the effects of the natural radiation environment on the shunt transistor is presented in this section. A detailed discussion of the radiation environment together with the radiation effects analysis and device selection criteria are presented in Reference 1. The selected MHT 8070 silicon NPN power transistor is not anticipated to be adversely affected by the environment. However, the effects of very low temperature operation on its radiation degradation characteristics should be further investigated.

5.3.1.2.1 Charged Particle Radiation Environment

The charged particle radiation environment that the spacecraft will encounter consists primarily of high energy electrons and protons trapped in the earth's magnetic field, solar cosmic radiation, and galactic cosmic rays. For the present assessment, the radiation environment data is taken from References 2 and 3. For the most part these radiation

environment specifications are essentially the same, differing only in their treatment of the available solar cosmic radiation data. The time integrated yearly flux of solar protons presented in Reference 2 is given in terms of a cumulative probability distribution assuming a log normal distribution for solar proton events which occurred during 1956 to 1963. The environment information presented in Reference 3, on the other hand, represents the total yearly integrated proton flux encountered in the year 1959. The proton dose received in this year was the highest proton dose received in consecutive calendar years over the 1956 to 1963 time period, and corresponds to about a 25 percent probability for the distribution functions given in Reference 2.

Since device sensitivity to radiation can be influenced by shielding, the effects of any inherent shielding surrounding the transistors should be considered. The internal radiation environment shown in Figure 5.3.1-4 takes shielding into account and is expressed in terms of the ionization dose in rads and an equivalent fission neutron dose per cm^2 (EFN/cm^2). This figure is based on the solar proton environment for the year 1959. The total ionization dose is useful in determining the extent of any radiation induced surface effects, while the equivalent neutron dose is used in determining the extent of radiation induced bulk damage. The equivalent fission neutron dose is used since the large majority of detailed radiation effects data for semiconductors have been obtained using reactor spectra. This equivalent dose is defined as that dose of fission neutrons which will cause the same amount of damage in semiconductors as the actual electron and proton environment. The anticipated current gain characteristics of the MHT 8070 transistor at the end of mission are shown in Figure 5.3.1-5. The data shown are the radiation degraded values of current gain at $35^{\circ}C$ over a range of initial gain for the environment given in Reference 3. It can be seen that the radiation characteristics of the device are more than adquate for use in the application for the specified radiation environment. The gain characteristics of the MHT 8070 at the end of

1. Tasca, D.M., "Radiation Effects on the Shunt Dissipator and Voltage Limiter", General Electric Company, PIR 1J85-314, July 12, 1968.

2. "Voyager Environmental Standards", JPI , September 25, 1967.

3. "Voyager Environmental Predictions", JPL, October 26, 1966.

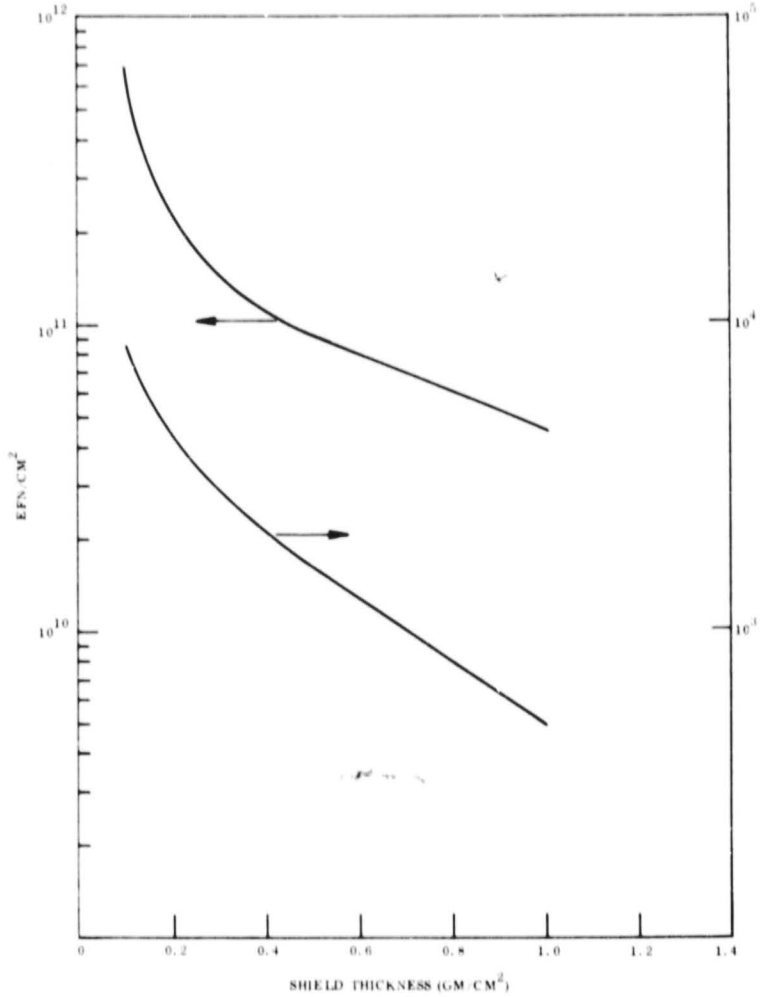


Figure 5.3.1-4 Total Mission Radiation Dose, Infinite Backshielding

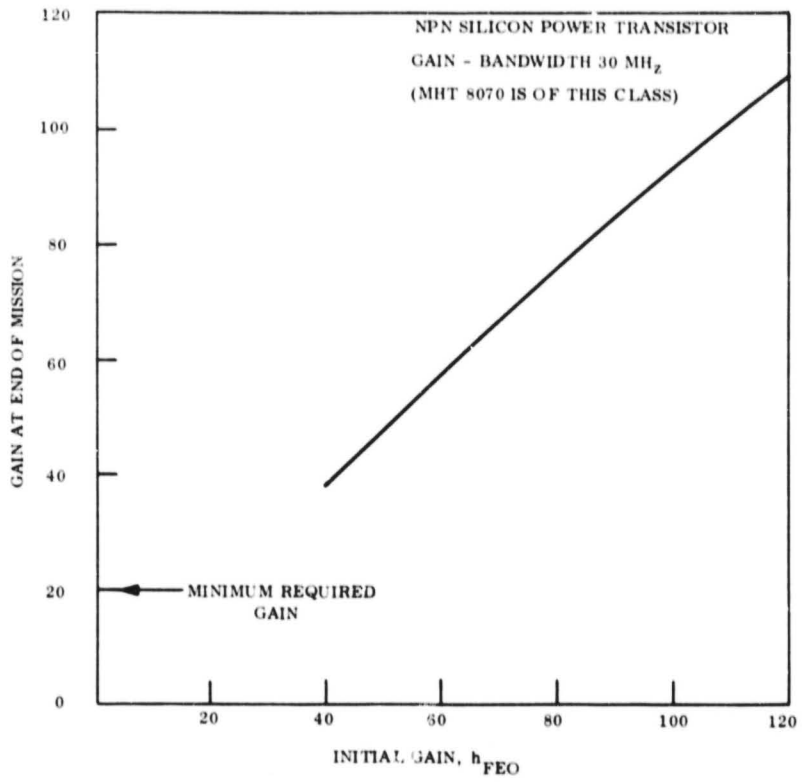


Figure 5.3.1-5 DC Current Gain Degradation, Silicon NPN Power Transistor

mission, when considering the solar proton environment defined in Reference 2, are shown in Figure 5.3.1-6. The data shown is presented in the form of the probability (in %) of the transistor gain at end of mission being less than or equal to that specified for three different values of initial gain. It can be seen that for probabilities of 10 percent or greater, the use of the MHT 8070 in the Power Subsystem would be adequate. For probabilities from 3 to 10 percent, the use of device selection techniques based on minimum acceptable initial gain would no doubt be required, while probabilities less than 3 percent would require selective shielding of the devices. A probability greater than 10 percent is considered to represent a reasonable estimate of the forthcoming solar maximum period. It should be noted that the gain degradation characteristics shown in Figures 5.3.1-5 and 5.3.1-6 were developed for a device ambient temperature of 35°C. Available information indicates that the radiation induced degradation in current gain increases with decreasing temperature. This data, however, is somewhat limited in that it was developed for small signal transistors and the range of temperatures investigated was only from 10°C to 60°C. Applying the data to the MHT 8070 indicates that the variations in gain degradation over the 10°C to 60°C range are minimal, though this might not be the case at -200°F. This aspect should be further investigated, although it is not expected to limit the usefulness of this device in the present application.

5.3.2 BATTERY CONSIDERATIONS

5.3.2.1 Requirements

Typical battery power requirements for a Mars orbiter mission are summarized in Table 5.3.2-1. The primary difference between the battery requirements for this mission and other Mariner missions is that battery power will be required at the time of planet encounter and also after encounter. This requirement may exist for one of two cases. In Case I power is required for solar eclipse periods during planetary orbit in addition to the orbit insertion and orbit trim maneuvers. The orbit cycle would be in the order of 12 to 24 hours with a 1 to 2 hour eclipse. The battery requirement could be from just a few to several hundred cycles, with the battery being charged during daylight periods by the solar array. However, with the long period of orbital time available before occultation occurs, it is not necessary that the batteries be operable in the cycling mode

Table 5.3.2-1. Battery Requirements

	Phase	Duration	Watt-hr Out	Depth of Discharge* (%)
CASE I	Prelaunch	10-0 Days	200	15
CASE I	Launch	45 Min	250	18.5
CASE I	Cruise I	**	-	-
CASE I	Maneuver	40 Min	270	20
CASE I	Cruise II	**	-	-
CASE I	Maneuver	40 Min	270	20
CASE I	Cruise III	**	-	-
CASE II	Orbit Insert	100 Min	675	50
CASE II	Recharge	24 Hr	-	-
CASE II	1st Orbit Trim	40 Min	270	20
CASE II	Recharge	24 Hr	-	-
CASE II	2nd Orbit Trim	40 Min	270	20
CASE II	Orbit Operations			
CASE II	No Eclipse	90 Days	-	-
CASE II	Eclipse	1.5 Hr	496	37
CASE II	Daylight	10.5 Hr (Total 90 Days)	-	-

* Based on 50 ah 27-volt battery (Mariner '69)
** Cruise I + II + III = 8 months

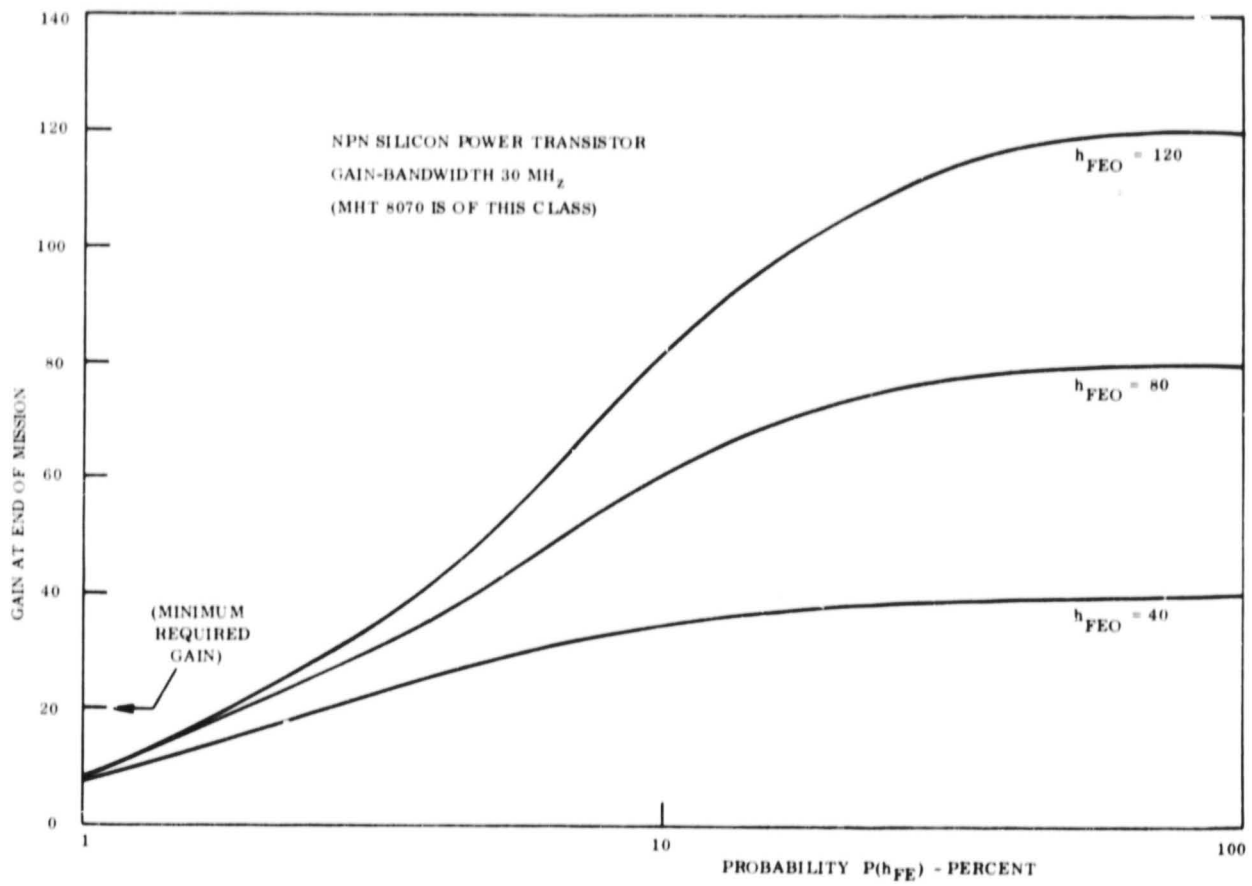


Figure 5.3.1-6 End of Mission Gain Probability

to ensure primary mission success. In other words, completion of the Case I requirements ensures a satisfactory mission.

5.3.2.2 Battery Candidates

There are three types of batteries which could be considered for use in the Mars vehicle power system. These batteries, all of the alkaline class, are secondary silver zinc, silver cadmium, and nickel cadmium.

The present Mariner battery is representative of a secondary silver-zinc battery and is an important contender in any future Mariner-type missions. Other silver-zinc batteries specifically designed for maximum cycle life with maximum energy density are also worthy of consideration. Consequently, GE-MSD initiated a test program two years ago to investigate the operating characteristics of such silver-zinc and silver-cadmium batteries.

Previous work carried out by GE-MSD and work performed by other investigators was believed extensive enough to develop the characteristics of standard nickel-cadmium cells and they were not included in the aforementioned test program. However, cells containing a new "third electrode" charge control device have been purchased recently and are being tested. Some of the highlights of the test program are reported here.

5.3.2.3 Silver-Zinc Cells

The silver-zinc cells have a nominal capacity of 50 ampere-hours and are assembled in Lustran (ABS) plastic cases with pressure gages attached. Each cell measures 6-1/8 inches high by 3-1/8 inches wide by 1-1/16 inches thick and weighs 1.55 pounds, exclusive of the pressure gage assembled to each cell. The 152 square inches of silver oxide is contained on 6 plates while the negative electrode consists of 7 zinc plates containing 2 percent mercuric oxide. Separation consists of two layers of polyvinyl alcohol and six layers of cellophane. Each cell contains 113cc of 40 percent KOH electrolyte. Cells were tested in packs of five and underwent charge and discharge characteristic tests, and 7- and 24-hour charge/discharge cycles. In addition, some cell packs were placed on float charge for several months and then subjected to repetitive cycling. A summary of tests on the silver-zinc cells is shown in Table 5.3.2-2. All cycle tests included a one hour discharge.

5.3.2.3.1 Charge Tests

To determine the most favorable charging procedure to use with these cells, the first part of the test program consisted of charge characterization tests. The charge regime selected was a constant current to a selected voltage limit, with the current tapering at this point holding the charge voltage at the selected level throughout the remainder of the charge period.

After several formation cycles, the pack was discharged a fixed amount (60, 40, or 20 percent of nominal capacity) and recharged to a specified voltage limit (1.96, 1.94, or 1.92 volts/cells, average). Maximum current levels were from 2 to 10 amps. Most of the charge tests were carried out at 75^{o}F, with a few at 30^{o}F for comparative purposes. The only difference attributable to the lower temperature was that charge acceptance was somewhat lower at low temperatures.

Table 5.3.2-2. Ag-Zn Test Summary

Pack No.	Months Test 1 2 3 4 5 6 7 8 9 10	Cycles to Failure
1-5	X Charge Tests	--
6-10	X 7 Hr. Cycle, 40% DOD	94
11-15	X 7 Hr Cycle, 20% DOD	314
16-20	X 24 Hr Cycle, 40% DOD	83
21-25	X 7 Mo. Float, 7 Hr Cycle, 20% DOD	169
26-30	X 24 Hr Cycle, 20% DOD	290
31-35	X Mars S/C Power Profile, 7 Hr Cycle 10% DOD	90
36-40	Float and Cycle at 30°F	Continuing

Typical data is plotted in Figure 5.3.2-1, where charge acceptance as a function of charge time is shown of three different voltage levels for a battery which had previously been discharged to a 60 percent depth of discharge.

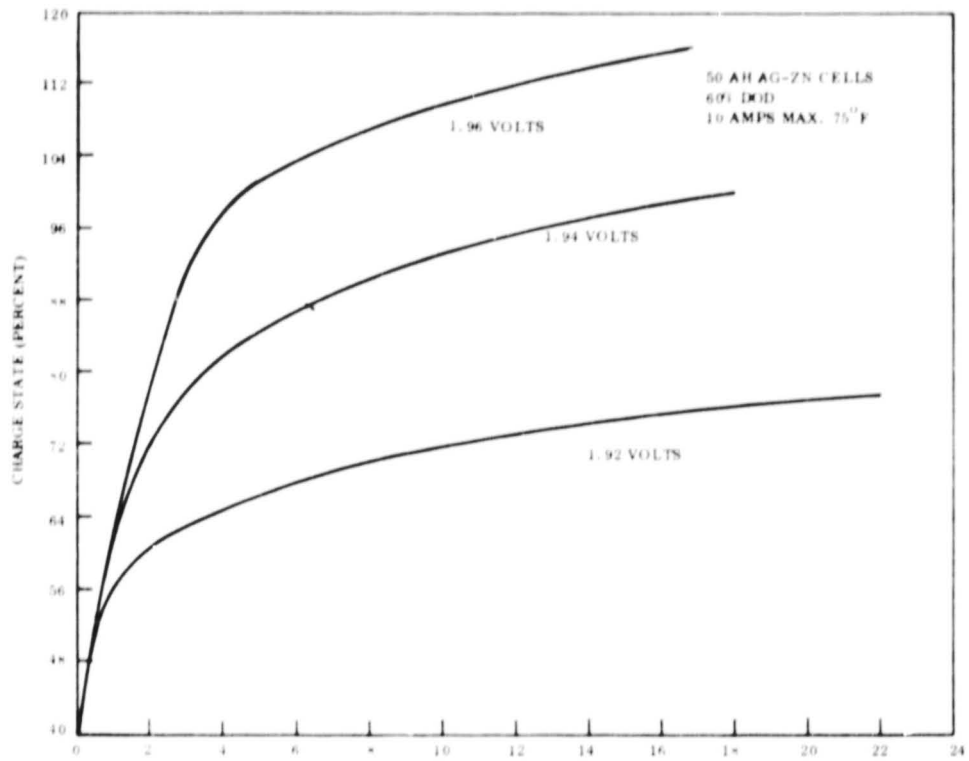


Figure 5.3.2-1 Ampere Hours Versus Charge Time

From these tests it was possible to determine the optimum charge voltage to use a function of depth of discharge and charge time. It was decided that an average voltage level of 1.92 volts per cell was generally too low to allow completion of the charge while a voltage level of 1.96 volts per cell frequently resulted in gas generation during the charge. The level of 1.94 volts was selected for charging, resulting in a limitation on the depth of discharge for shorter cycles.

The charge data may be represented in another way as shown in Figure 5.3.2-2. Here the point at which tapering of the current occurs is plotted as a function of the charge current. The curve is valid for a cell voltage limit of 1.94 volts per cell. The plot shows the time necessary to complete the charge from a given depth of discharge. In Case A, a 2- amp rate is used as the maximum charge current. Starting from a 50 percent depth of discharge (DOD) it can be seen that 15 ampere-hours may be returned in 7.5 hours reducing the DOD to 20 percent; to complete the charge requires an additional 14.5 hours.

A close study of the data presented in Figure 5.3.2-2 suggests that it might be advisable to operate the battery at less than full charge. Suppose that it is desired to remove 15 ampere-hours of capacity from the battery. Case A shows that in operating between 20 and 50 percent DOD, the 15 ampere-hours could be returned to the battery in 7.5 hours, while Case B shows that trying to return this 15 ampere-hours to a battery operating between 30 percent DOD and full charge would require 17.5 hours. It must be assured that cycle life does not suffer from the fact that the battery is operating from less than a fully charged condition.

5.3.2.3.2 Discharge Tests

A set of typical V-I curves was generated for this cell by discharging the cell at various rates and measuring the corresponding stabilized voltage. Data is shown in Figure 5.3.2-3 for temperatures of 40, 75, and 90°F.

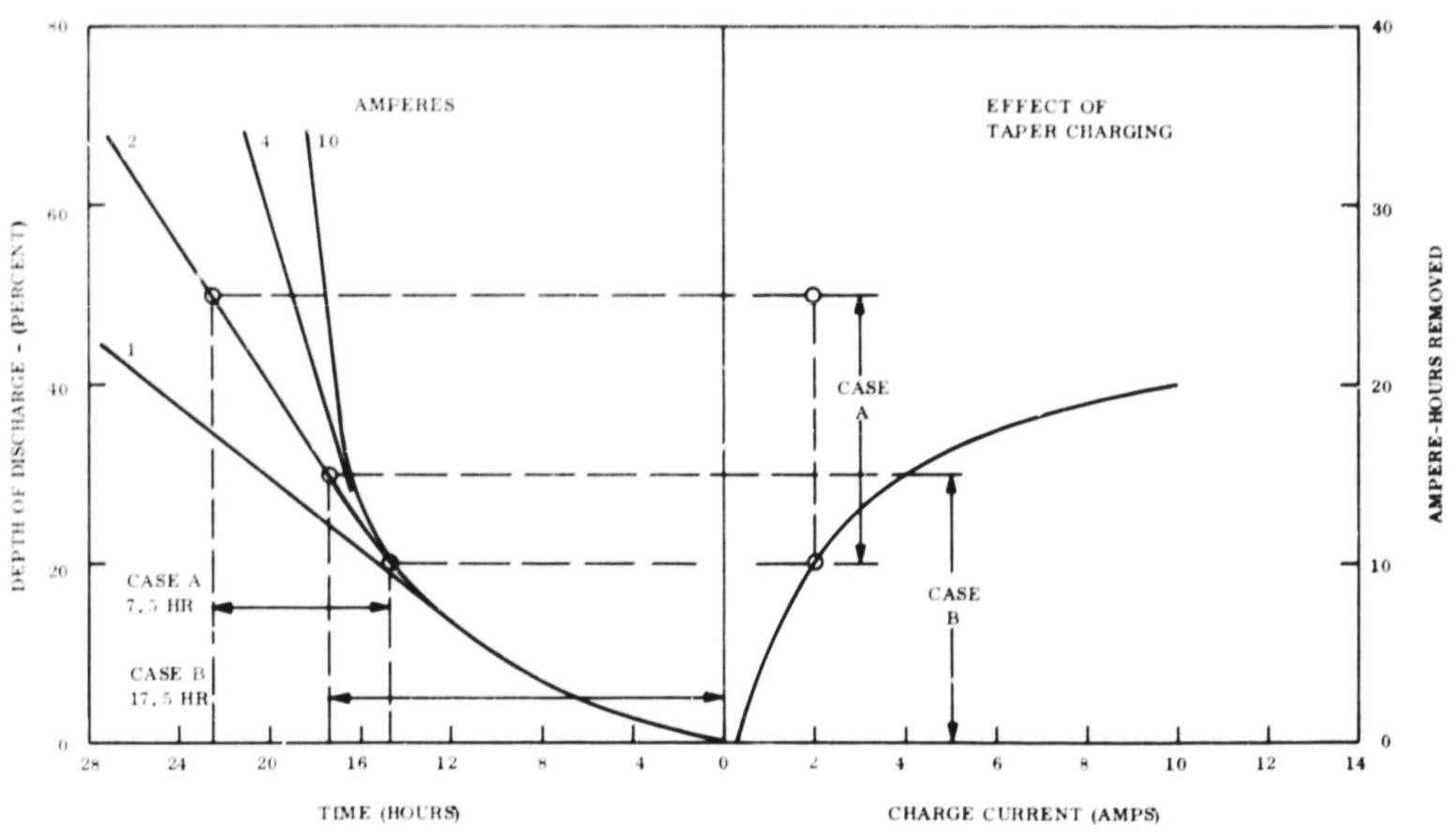


Figure 5.3.2-2. Charging Characteristics 50 AH, Ag-Zn Cells, 1.94 Volts/Cell Limit

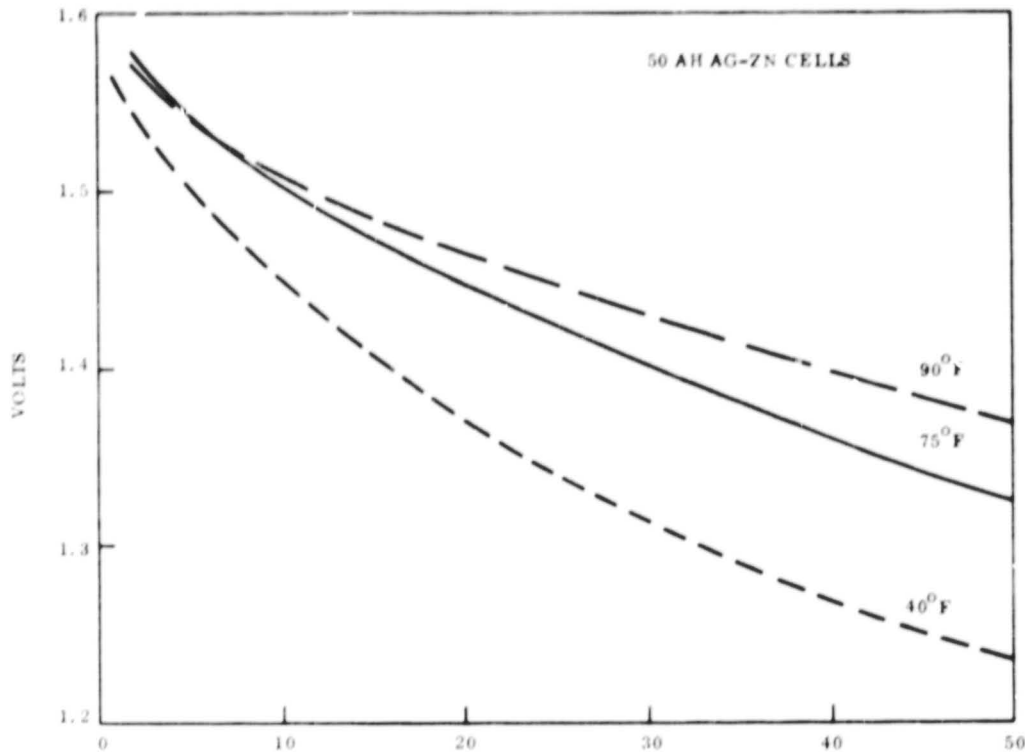


Figure 5.3.2-3. Volts Versus Discharge Rate

5.3.2.3.3 Cycle Tests

Cells packs were put on automatic 7- and 24-hour cycles at room ambient conditions discharging to a 20 or 40 percent depth of discharge. The results of the tests are summarized in Table 5.3.2-2. When comparing the results of the tests, it may be noted that the total life of the battery pack appears to be a function of the number of cycles rather than the time on test. Compare the 40 percent DOD tests (94, 7-hour cycles and 83, 24-hour cycles) with the 20 percent DOD tests (314, 7-hour cycles and 290, 24-hour cycles). While the results of the 40 percent DOD tests are disappointing, the 20 percent DOD tests are encouraging, especially when it is recalled that this silver-zinc cell at a 15 percent DOD is equivalent in usable energy density to a nickel-cadmium cell at a 60 percent DOD.

Plots of average end-of-discharge voltage versus cycle number are shown in Figure 5.3.2-4 for the 20 percent DOD 7-hour cycle and in Figure 5.3.2-5 for the 20 percent DOD 24-hour cycle.

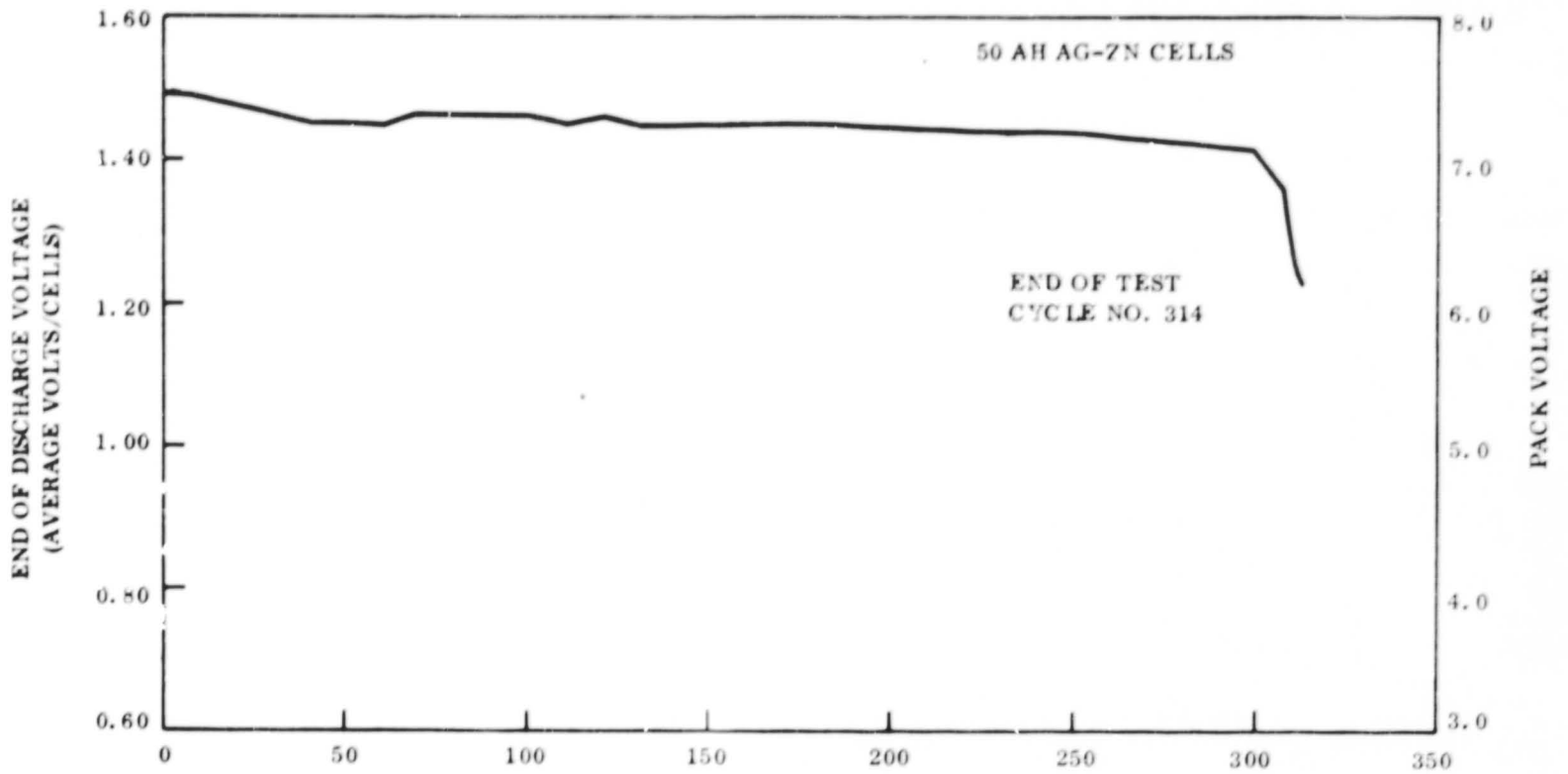


Figure 5.3.2-4 End Discharge Voltage Versus Cycle, 20 Percent DOD, 7-Hour Cycle

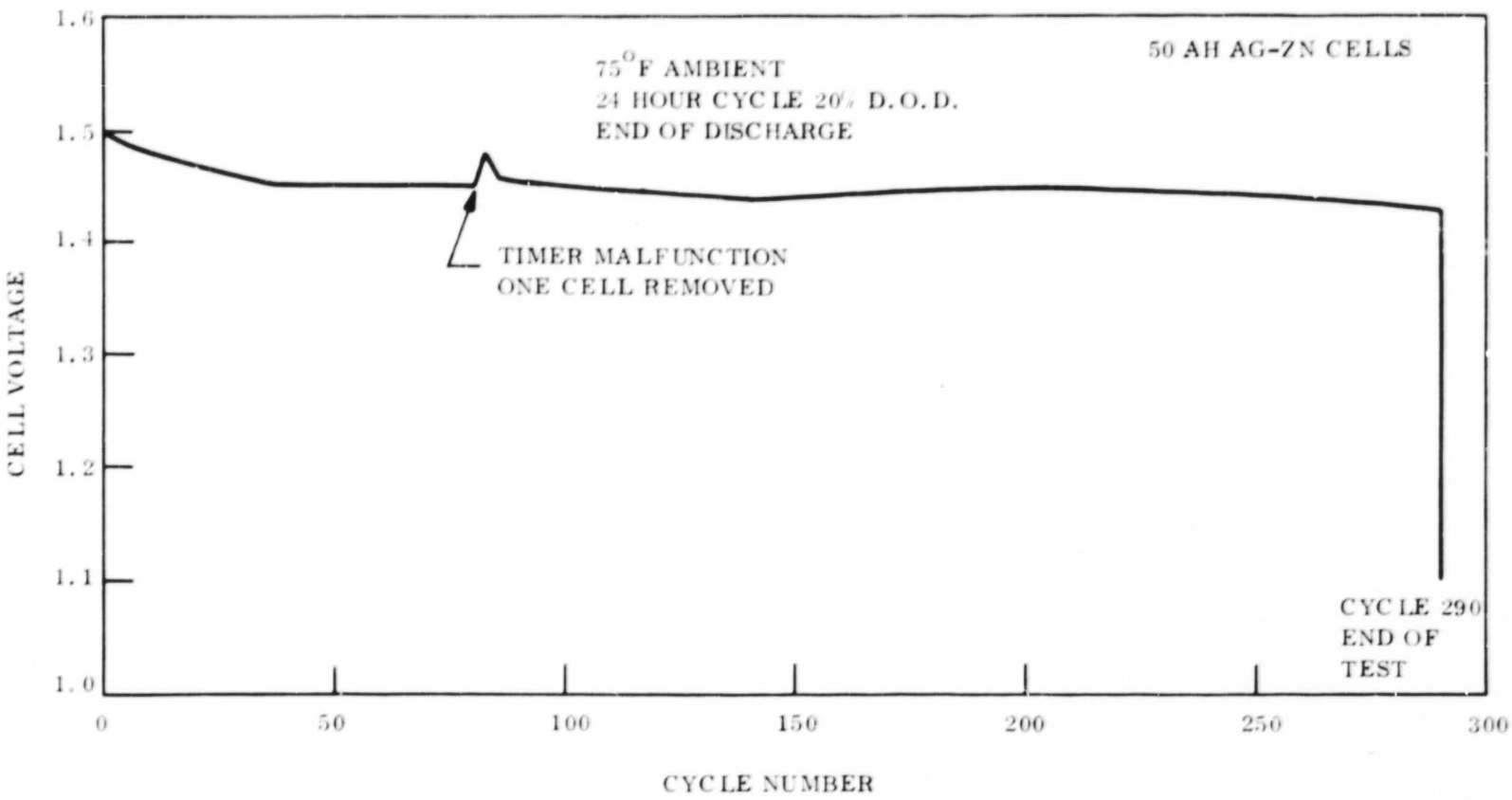


Figure 5.3.2-5. Pack 811-26 to 30, 5-50 AH Ag-Zn Cells

In all cases, silver-zinc cell failure was caused by internal cell shorting. Because of the use of a relatively low charge voltage limit, 1.94 volts/cell, cell gassing was not a problem and cells did not leak or dry out. Also the polyvinyl alcohol, coupled with the cellophane separator system virtually eliminated the problem of silver migration. Failure was eventually caused by solution and precipitation of the negative material until the separator was either punctured or bypassed.

5.3.2.3.4 Float Tests

Pack 811-21 to 25 was floated in a fully charged condition at an average voltage level of 1.87 volts/cell for 7 months. Following the float period, the pack was put on a 7-hour cycle at a 20 percent DOD. Figure 5.3.2-6 shows the results of several capacity discharges of this pack. It may be seen that the total capacity of the pack was not appreciably degraded; however, when placed on cycle test, the pack failed after only 169, 20-percent DOD cycles as compared to 314 cycles for a pack which had not undergone the float period. Upon inspection of the failed cells, it was observed that the PVA separator had degraded considerably and this was believed to be the reason for the decreased cycle life.

Additional packs were placed on a float and cycle test profile more nearly simulating the actual Mars spacecraft mission, including periodic discharge during the float period. One of these packs, 811-31 to 36, was cycled at a 10 percent DOD on a 7-hour cycle to determine if the depth of discharge had an appreciable effect on cycle life. When this pack failed after about 90 cycles and these results were compared with pack 811-21 to 25 which lasted for 169 cycles at 20 percent DOD following the float period, it was decided that the life limiting parameter was the total time on test.

Pack 811-36 to 40 is continuing on the float test at 30^{o}F to determine the effect on life of floating silver-zinc cells at low temperatures.

5.3.2.4 Silver-Cadmium Cells

The silver-cadmium cells have a nominal capacity of 20 ampere-hours and are assembled in type 302 stainless steel cans. Each cell has two ceramic bushings, insulating the negative and

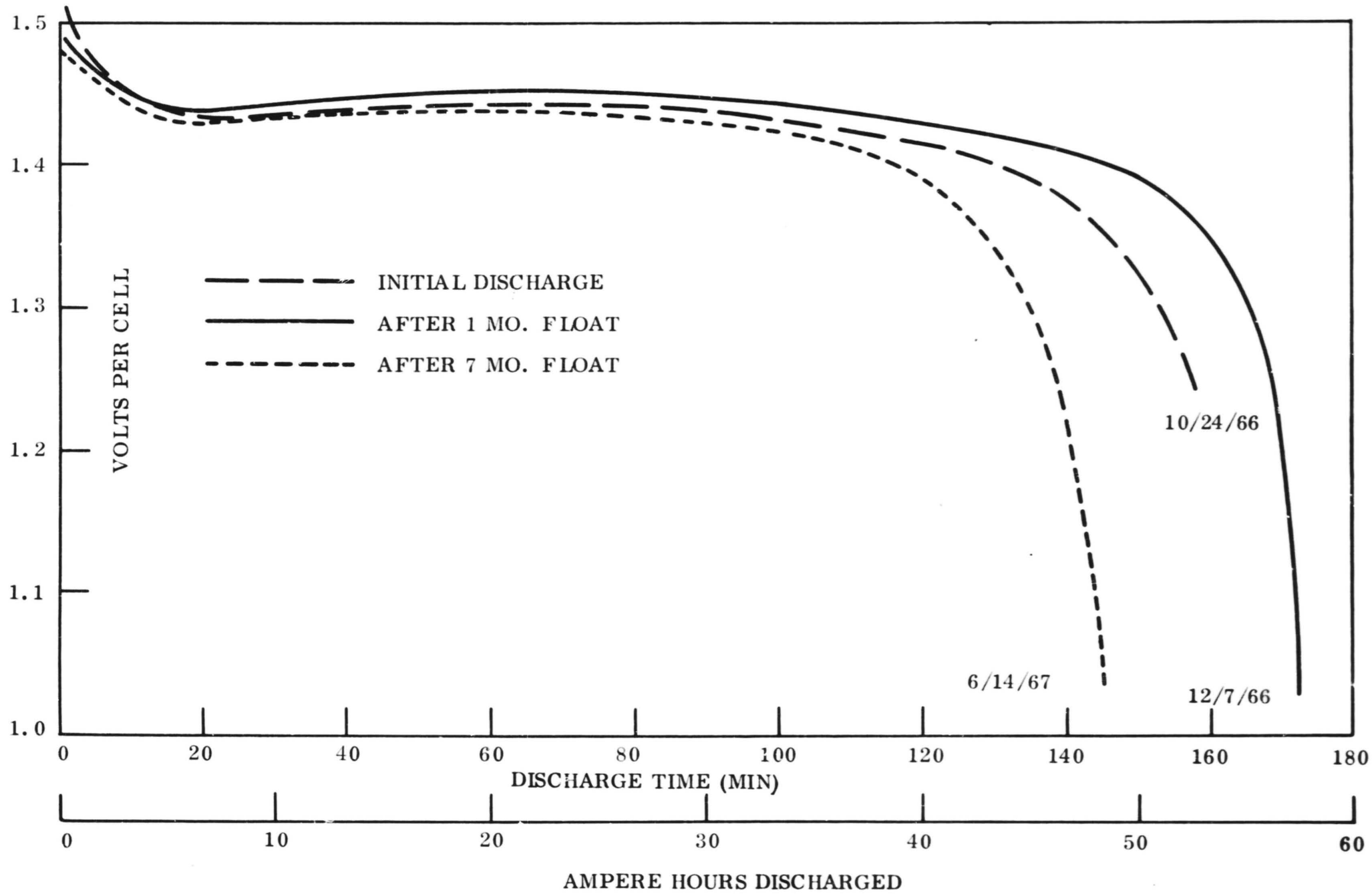


Figure 5.3.2-6. Silver-Zinc Secondary Cells Discharge Volts Versus Time for 20 Amp Discharge

positive terminals from the case. Each cell measures 3-7/16 inches high by 3-3/16 inches wide by 1-7/16 inches in thickness and weights 1.5 pounds, exclusive of the pressure gage. The 154 square inches of silver oxide is contained on 12 plates while 13 plates contain the negative cadmium material. Separation consists of two layers of polyvinyl alcohol and four layers of cellophane. The electrolyte, in all cases but one, consists of 93 cc of 30 percent KOH. Pack F contains 80 cc of 40 percent KOH.

Cells were tested in packs of six to determine charge and discharge characteristics and cycling capability on 7- and 24-hour charge/discharge cycles. In addition, one pack was placed on float to determine cycling capability after an extended period of floating in a fully charged condition. A summary of the silver cadmium tests is shown in Table 5.3.2-3

Table 5.3.2-3. Ag-Cd Test Summary

Pack No.	Months Test 1 2 3 4 5 6 7 8 9 10 11	Cycles To Failure
A	Charge Tests | 7 Mo Float | X 7 Hr Cycle 20%DOD	97
B	X 7 Hr Cycle, 40% DOD	285
C	X 24 Hr Cycle, 60% DOD	126
D	X 24 Hr Cycle, 40% DOD	135
E	X 7 Hr Cycle, 20% DOD	705
F	X 7 Hr Cycle 40% DOD 40%KOH, 2 Step Charge	1100

5.3.2.4.1 Charge Tests

Charge tests, similar to tests carried out on the silver-zinc cells, were also performed on the silver-cadmium cells. Voltage levels of 1.48, 1.50, and 1.52 volts/cell average were used, recharging from 60, 40, and 20 percent depth of discharge. A 3.0 amp maximum rate was used in all cases. All of the charge tests on the silver-cadmium cells were conducted at room ambient, about 75°F. Data was obtained similar to that obtained for the silver-zinc cells. It was determined that 1.48 volts/cell was too low for efficient charging, but that 1.50 or 1.52 volts/cell would be satisfactory, if the depth of discharge is not too great. Under certain conditions (pack F) 1.54 volts/cell was used satisfactorily, but usually this voltage level resulted in severe unbalancing during charging with the result that gassing occurred in some cells in the test pack.

5.3.2.4.2 Discharge Tests

Silver-cadmium cells were discharged at 40, 75, and 90°F to generate typical V-I curves. The results are shown in Figure 5.2.2-7 where data is plotted for rates of 1 to 20 amps.

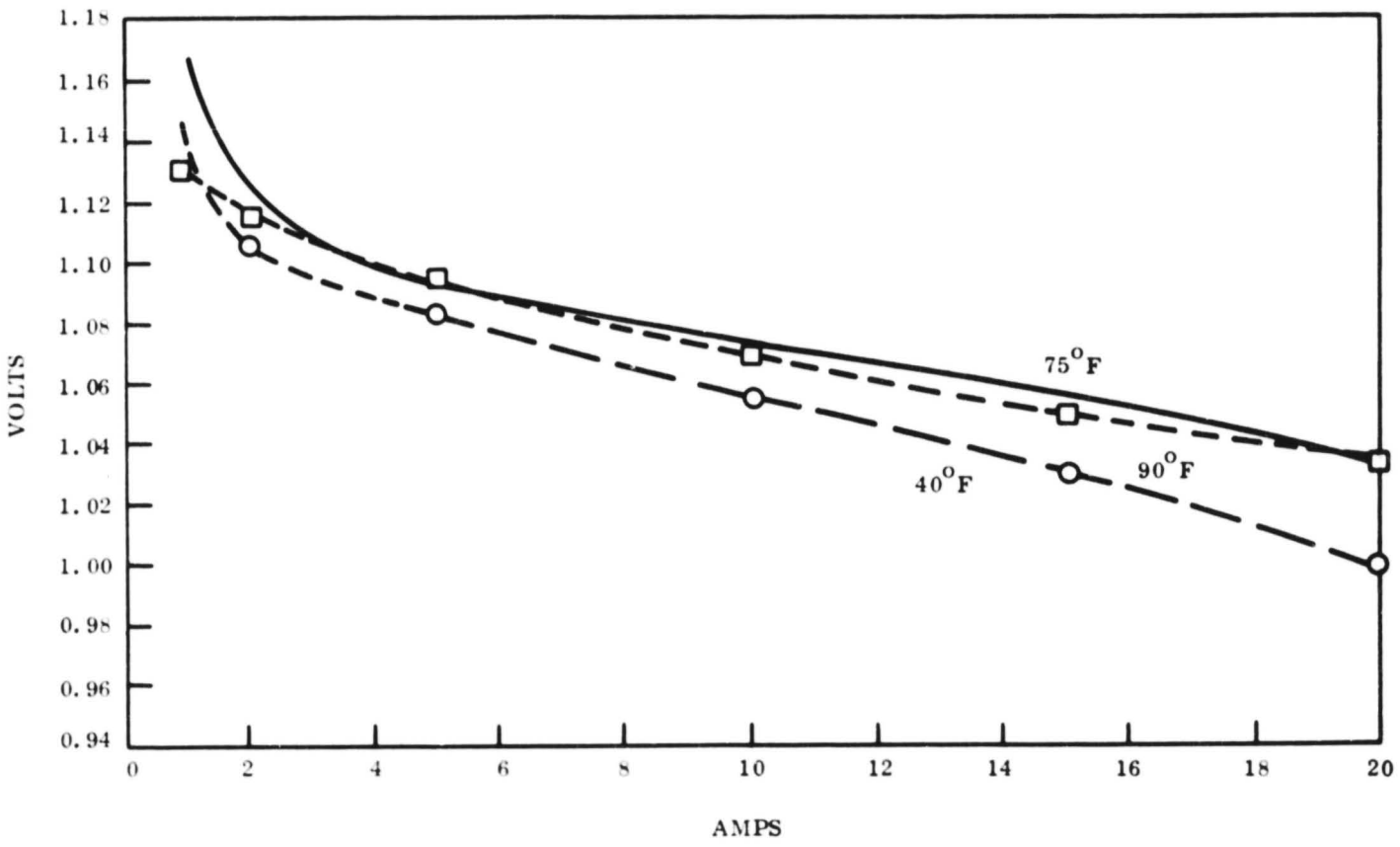


Figure 5.3.2-7. Volts Versus Discharge Rate for 20 AH Silver-Cadmium Sealed Cells

5.3.2.4.3 Cycle Tests

Packs were put on 24-hour cycles at 60 and 40 percent DOD and on 7-hour cycles at 40 and 20 percent DOD. Results of these tests are summarized in Table 5.3.2-3. No correlation of cycle life with depth of discharge or cycle period is possible, however, cycle life was disappointingly poor except for pack F.

Considering that the nominal energy density is only about 14 watt-hours per pound, these cells would not be competitive with nickel-cadmium cells unless a definite magnetic cleanliness requirement existed.

All silver-cadmium cells failed by a low end-of-discharge voltage phenomenon. When the end-of-charge voltage was increased to increase the charge input, cell unbalancing occurred resulting in gas generation in some of the cells. Failure analysis showed no signs of internal shorting or silver migration. From this it was deduced that failure was caused by negative plate fading or passivation. This phenomena was discussed with the manufacturer who concurred in the explanation, because the negative plate was of pasted construction rather than impregnated on a sintered nickel substrate.

Pack F behaved quite differently from the other silver cadmium test packs. It survived over 1100 cycles at 40 percent DOD on a 7-hour cycle. Figure 5.3.2-8 shows the end of discharge voltage versus cycle number. It is significant to note that failure was caused by a low end-of-discharge voltage and no shorts were in evidence from the failure analysis. The results of this test suggest areas of interest for future investigations of silver cadmium cells. The reason for the improved operation can be explained by any one of three unique factors existing for this pack:

a. By an extremely fortunate set of circumstances, six well-balanced cells were selected that can be operated at a charge voltage equivalent to 1.54 volts per cell without becoming unbalanced and generating gas.

b. The inception of a two-step voltage limit causes the charge voltage to drop to a safe value before unbalancing occurs. Operation in this mode is illustrated by Figure 5.3.2.9, where the upper voltage level of 1.54 volts per cell is maintained until the charge current decays to 0.21 amp. At this point the cell voltage is reduced to an average of 1.42 volts/cell, just above the open circuit voltage.

c. The cells were filled with 40 percent KOH rather than 30 percent KOH electrolyte, resulting in less severe fading and degradation.

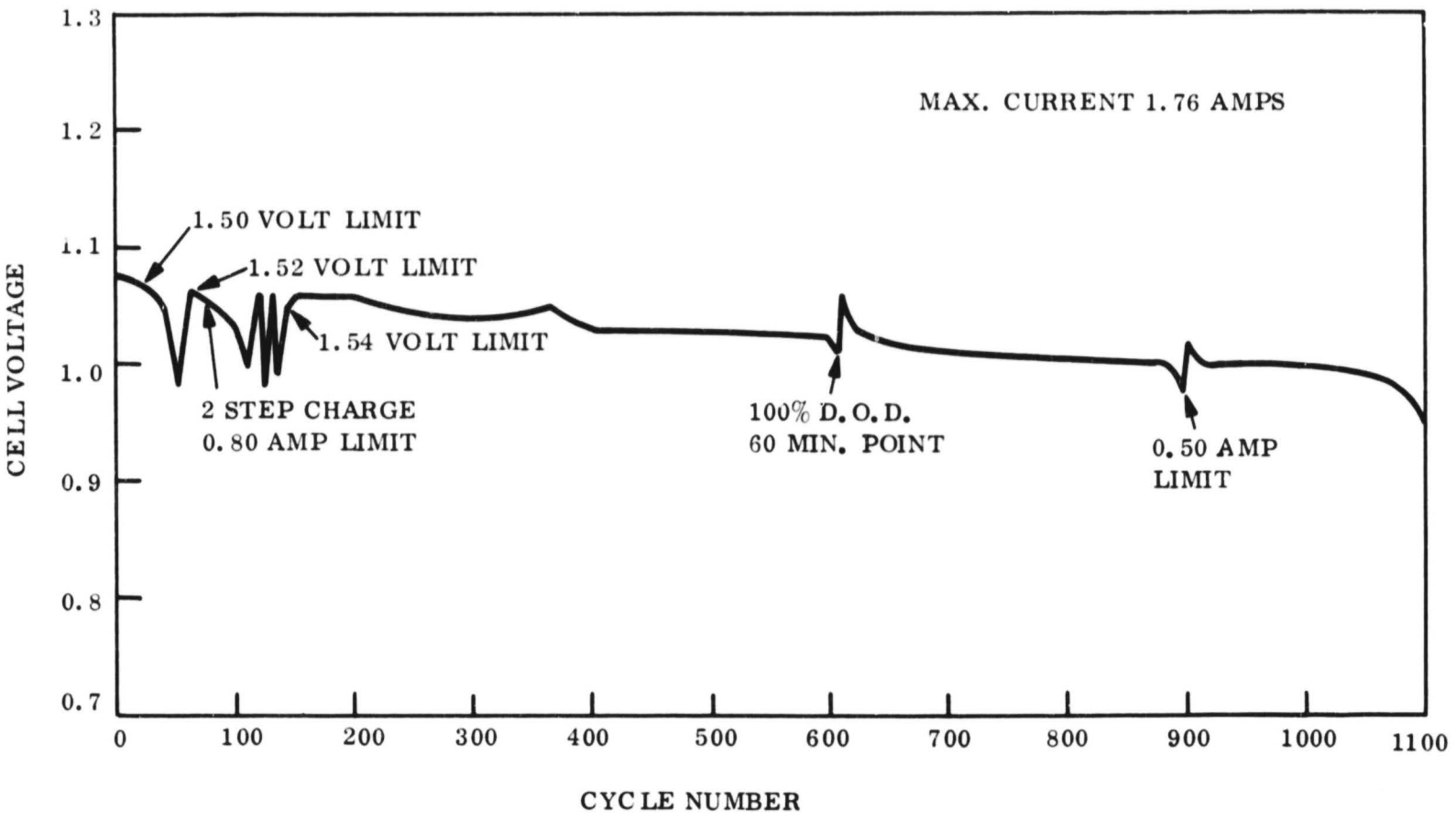


Figure 5.3.2-8. Pack F 6,20 AH Ag-Cd Cells 7-Hr Cycle, 40 Percent DOD, 75°F End-of-Discharge

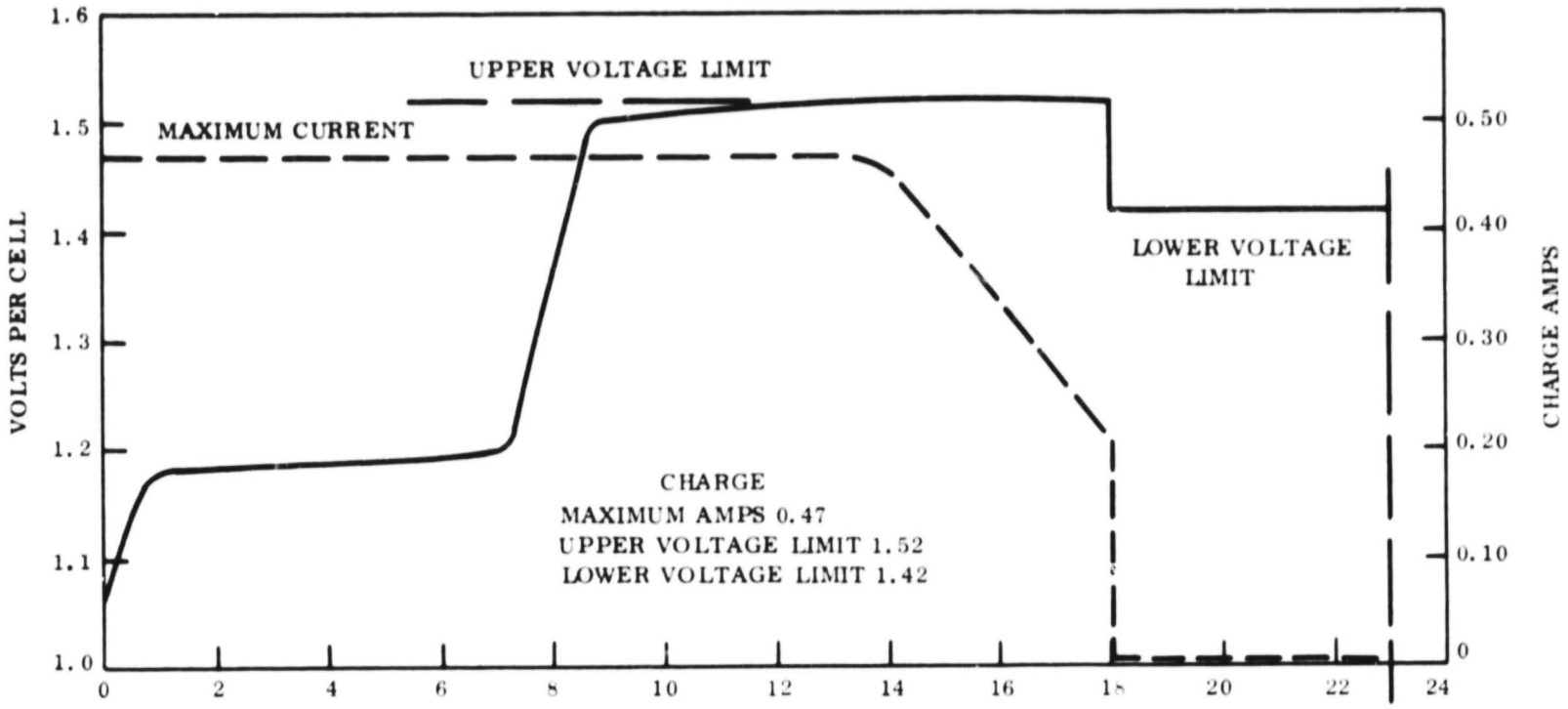


Figure 5.3.2-9. Silver-Cadmium Cell Pack D Cycle 109, 40 Percent DOD, 24-Hr Cycle

5.3.2.4.4 Float Tests

One pack was placed on a 7-month float at 1.42 volts/cell and then cycled at a 20 percent depth of discharge on a 7-hour cycle. The pack survived only 97 cycles before failure occurred as a result of the inability to accept a charge. It was concluded that this cell is severely penalized by long periods on float charge and would not be satisfactory for a Mariner-type mission.

5.3.2.5 Nickel-Cadmium Cells

General Electric Missile and Space Division has carried out a considerable amount of testing with hermetically sealed nickel-cadmium cells. Batteries have been tested in thermal-vacuum chambers to determine thermal characteristics, on 5-hour and synchronous orbit-type cycles to determine cycle life capability, and on continuous overcharge tests.

Cells used for the latter tests were 12 ampere-hour cells, purchased in late 1961, which were placed on a continuous charge for over 500 days at a C/7 rate and following a capacity discharge, when they delivered over 12 ampere hours of capacity, were put in storage in the laboratory for over two years. They were subsequently removed from storage, given a few conditioning cycles, and placed on a continuous 24-hour cycle, discharging to a 60 percent DOD. These cells completed 666 cycles before being taken off test because of low end-of-discharge voltage.

5.3.2.5.1 Third Electrode Nickel-Cadmium Cells

A relatively new method in battery charge controls employs the use of a third or auxiliary electrode to signal when a cell has reached full charge. Using this method, a nickel-cadmium battery may be recharged at a rapid rate and reduced to a safe trickle rate when the charge has been completed. Several 20 ampere-hour cells containing third electrodes have been procured for evaluation. It is expected that they will be tested at several charge rates and temperatures to determine the effect of these parameters on the third electrode signal and the charge acceptance of the cells.

An overall comparison of silver-zinc, silver-cadmium, and nickel-cadmium cycle-life capability as a function of depth-of-discharge is shown in Figure 5.3.2-10.

5.3.2.6 Mariner '69 Battery

The Mariner '64 battery is completely described in JPL Technical Report No. 32-854 and may be identified as Electric Storage Battery Co. Model #257. The Mariner '69 battery will be essentially the same battery as was used on the '64 vehicle, but incorporating manufacturing improvements for increased life capability.

The battery was sealed and contained 18 cells with a nominal capacity of 50 ampere hours. The gross weight of the battery package was about 34 pounds, resulting in a capacity of 1350 watt-hours and an energy density of about 40 watt-hours per pound at a 10 amp discharge rate.

5.3.2.6.1 Charging

The Mariner '64 battery was charged at a rate of 300 milliamperes to a voltage limit of 34.6 volts (1.93 volts/cell) until the current dropped to 20 milliamperes. At this point, the charger was turned off. However, a trickle charge of 1.5 milliamperes remained on continuously because of telemetry required for a voltage transducer. The result was that battery voltage continued to increase and several of the cells developed shorts before the mission was terminated.

It is planned to modify the '69 charge regime to eliminate the telemetry power drain so that the battery may be carried in a completely open-circuited mode.

5.3.2.6.2 Test Results

According to information from the Electric Storage Battery Company (ESB), new Mariner-type batteries have been cycled to 100 percent DOD for 50 cycles at a 10-amp discharge rate and have delivered rated capacity. In addition, it has been determined by ESB that the battery will sustain a 7- to 9-month stand and still deliver the rated 50 ampere-hours of capacity. However, no attempts have been made to cycle the battery after the stand period.

A test program is being originated at Crane, Indiana, where secondary silver-zinc batteries from different manufacturers will be cycled at several depths of discharge after various stand periods and at various temperatures. These tests should be followed carefully to verify the adaptability of the silver-zinc battery to an orbiter mission profile. In addition, a comparison should be made between batteries which have remained on float charge during the trans-Mars period and those which have been held open circuited in the charged condition. The effect of this variable on cycle life as well as capacity should be determined. It is important that some of the Mariner-type batteries with improved separation be included in the float and cycle tests to determine if this battery would be suitable for the orbiter type mission. It is also suggested that the possibility of operating the Mariner battery in a vented or pressure relieved mode be investigated. The vented cell

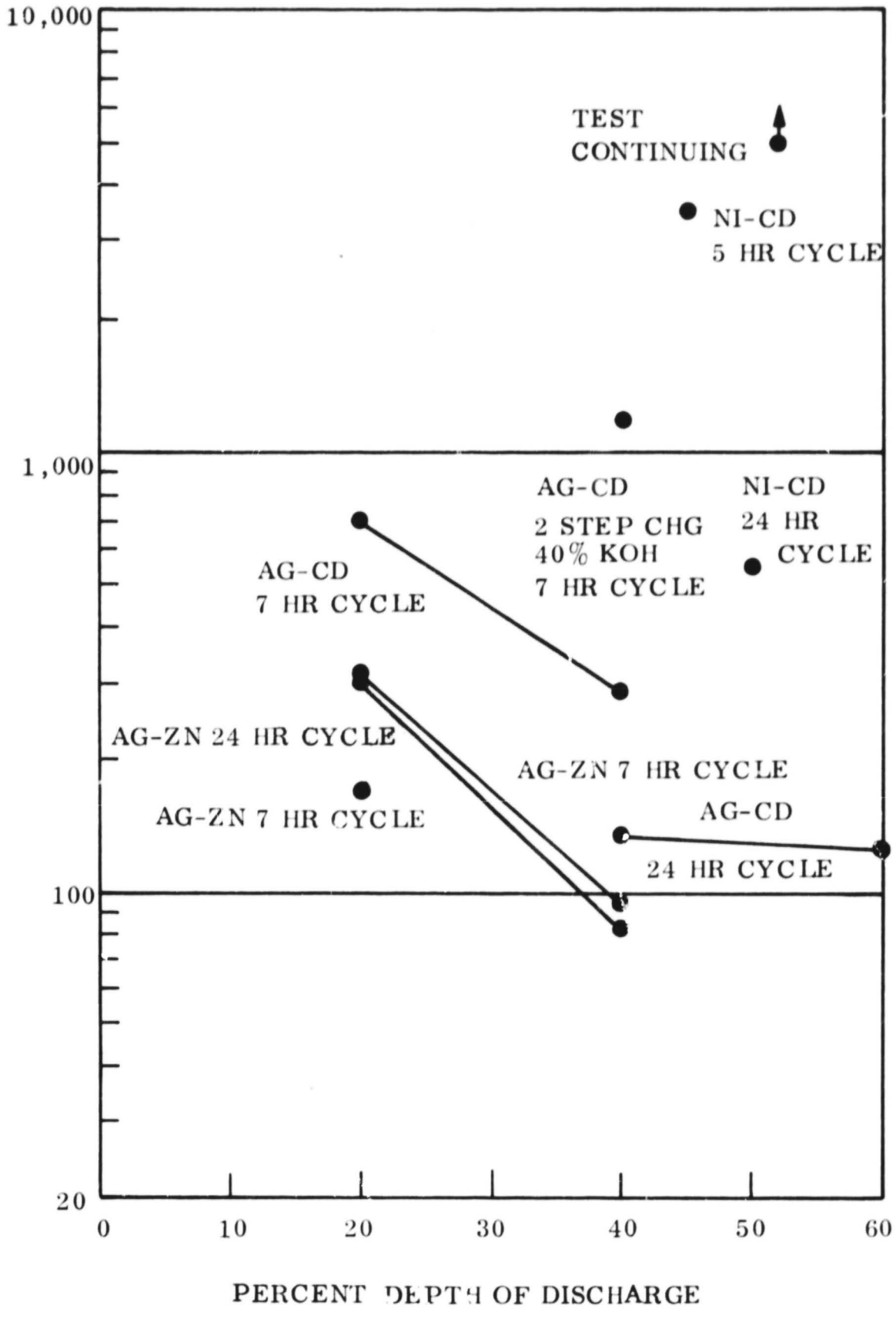


Figure 5.3.2-10 Cycle Life Versus DOD for Ag-Zn, Ag-Cd, and Ni-Cd Cells at 25°C

has shown the capability of operating for extended periods of time, eliminating the problem of excessive gas pressure which may build up within the battery during periods of trickle charge. Obviously, gas venting cannot be excessive or the battery will dry out causing a loss in capacity.

5.3.2.7 Battery Comparison

Four battery types have been considered in the previous paragraphs for use in the Mars vehicle. Based on mission requirements and information available on their present states of development, the battery used on the Mariner '64 spacecraft would be the preferred selection. This decision is based primarily on the relatively high energy density of the system, the absence of specific cyclic operation during the orbit phase, and the fact that the battery has been flight proven on previous Mariner missions. A comparison of battery characteristics is shown in Table 5.3.2-4.

Table 5.3.2-4. Battery Characteristics

	Battery Type			
	Mariner Ag-Zn	Vented Ag-Zn	Ag-Cd	NiCd
Energy Density, w-hr/lb	40	40	14	10
Relative Weight	1	1	3	3.3
Relative Volume	1	1	2	2
Cycling Capability	50	50-100	100-1000	>1000
Float Capability	?	Fair	Fair	Good
Flight Tested	Yes	No	No	Yes
Sealed	Yes	No	Yes	Yes
Trickle Charge Req'd	No	No	No	Yes
Nonmagnetic	Yes	Yes	Yes	No

SECTION 6

CONCLUSIONS AND RECOMMENDATIONS

Detailed conclusions and recommendations are made throughout the report. This section presents the major summary conclusions and recommendations.

6.1 CONCLUSIONS

The major conclusions of the study are as follows:

a. A shunt system, as described in Section 4, appears to offer a power system which will meet flyby and orbiter missions of the type studied with improved efficiency and reliability.

b. The array/battery sharing mode of operation for the MM'69 type power system makes operation more sensitive in the orbiting missions under array limited conditions. This sensitivity limits the operational flexibility and requires more margin to assure that operation does not become array power limited.

c. One major difference between the flyby and orbiting mission is the non-time criticality of the science loads in the orbiter missions. This fact has important implications for the design of the power system distribution and control for any type power system.

d. The application of redundancy should be kept as simple as possible because of its complex interplay with fault protection, sensing, and switching. Beyond the simplest implementation concepts, it becomes increasingly difficult to ascertain that all significant interactions have been identified.

6.2 RECOMMENDATIONS

a. Consideration should be given to using separate relays on the science loads for orbiting missions -- independent of the type power system used.

b. The existing sensitivity of the MM'69 type power system to array/battery sharing operation for orbiting missions should be carefully evaluated both experimentally and analytically.

c. The Phase I shunt system design appears to offer significant efficiency and reliability improvements and should be further developed on a Phase II effort.